Tests of small X-ray Active Matrix Pixel Sensor prototypes at the National Synchrotron Light Source

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Outline

- Motivation and Detector Initial Requirements.
- Detector Principle / Fundamental Design.
- X-ray Active Matrix Pixel Sensor (XAMPS).
- Device fabrication.
- Tests results.
- Future development.

Linac Coherent Light Source (LCLS)

- LCLS is a X-ray free-electron laser being built at Stanford (2009).
- Photons energy 800 eV – 8 keV.
- Pulses ~ 100 fs at 120 Hz.

Motivation: having a source with atomic-scale time and wavelength (*and enough photons to "take dynamic pictures of materials" in one shot*).

http://www-ssrl.slac.stanford.edu/lcls/

X-ray Pump Probe Instrument

- Ultrafast optical laser pulse: to excite changes in atoms positions
- LCLS X-ray pulses: to study diffraction from the excited sample
- Detector: to study X-ray scattering pattern or X-ray absorption and emission

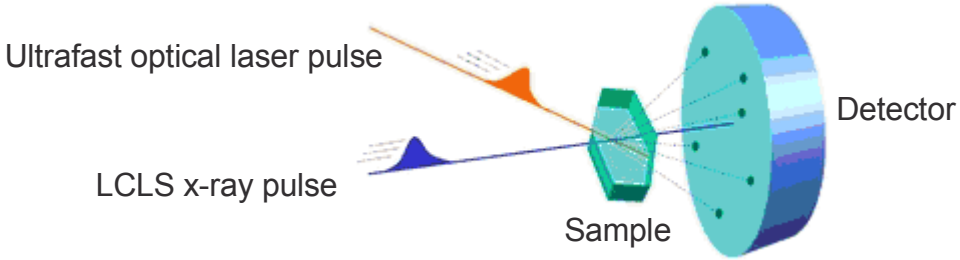
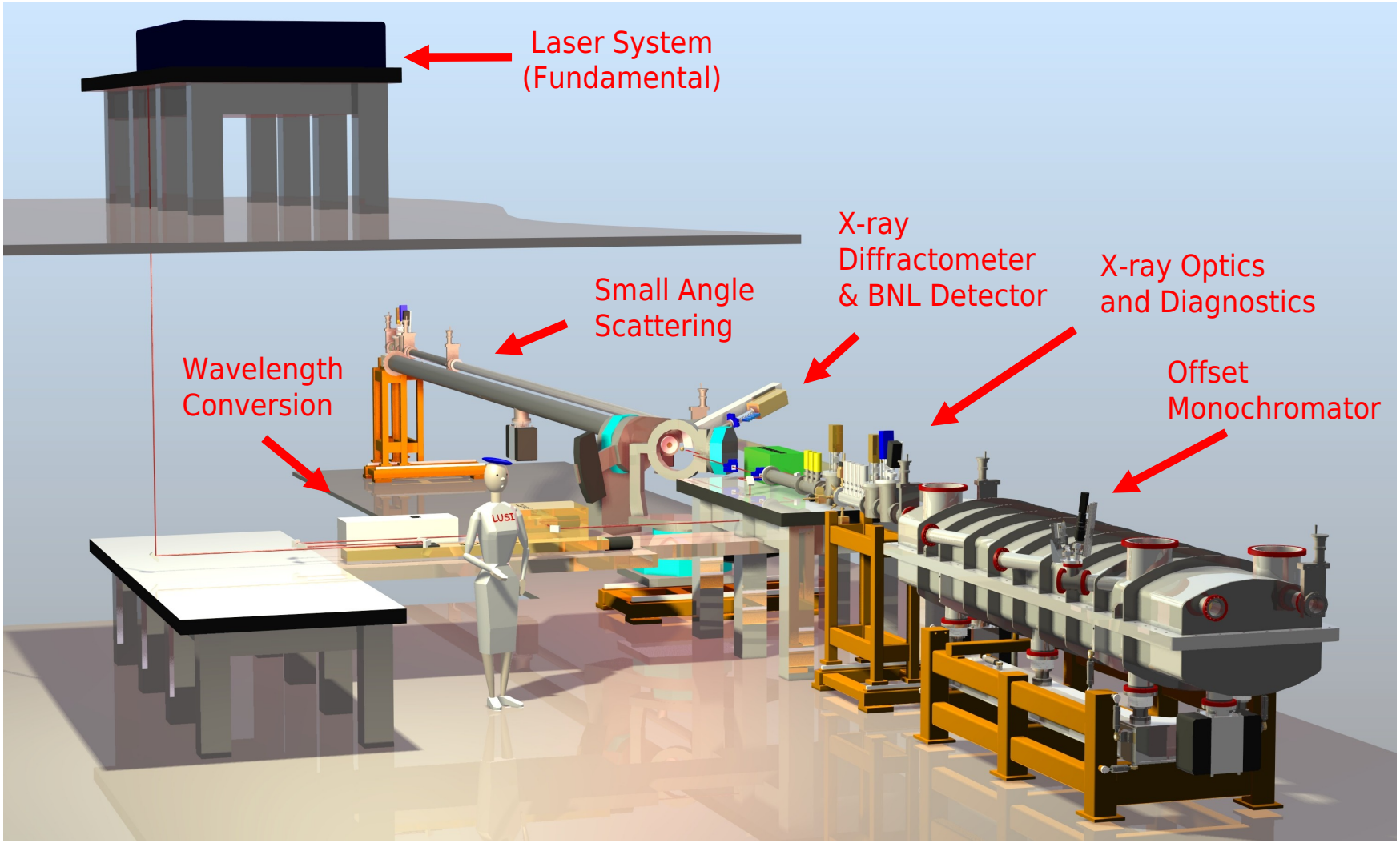


Figure courtesy of the Centre for Molecular Movies, established by the Danish National Research Foundation.

http://photonscience.slac.stanford.edu/lusi/instruments/xpp.php

X-ray Pump Probe Instrument



David Fritz, SLAC-LUSI

Fast readout imaging detector

- Integrating detector because of the nature of the experiment.
- Single photon sensitivity.
- Large dynamic range: 10^4 photons full-well.
- Low noise: better than 1 photon.
- Readout time better than 8 ms.
- 1024 x1024 pixels.
- Photon energy: 8 keV.

XAMPS: simplest structure

- Monolithic devices built on fully-depleted high-resistivity silicon.
- Highly efficient with 100% fill factor.
- Switching mechanism integrated with sensor.
- Row-by-row parallel readout by off-sensor amplifiers (N readout channels instead of N x N, modular readout from edge of detector by a few ~16 small ASICs).
- Small pixels in principle possible (no on-pixel amps or small 3T design).

W. Chen *et al*. IEEE Trans. Nucl. Sci. 49 (3) (2002) 1006.

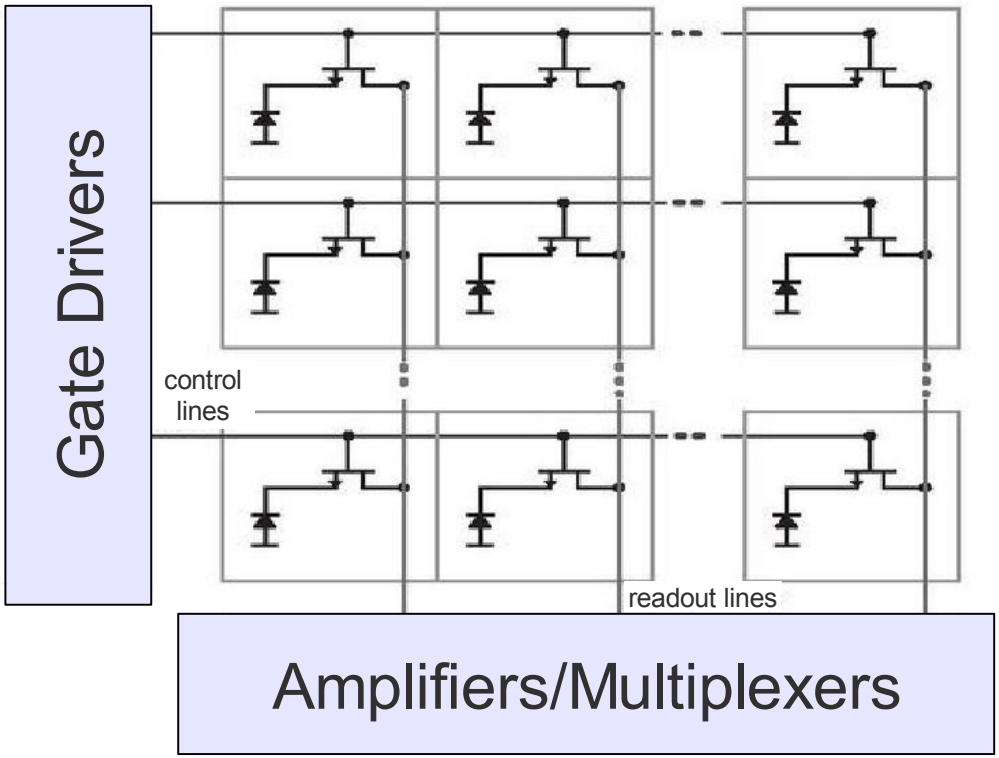
W. Chen *et al.* Nucl. Instr. Meth. A 512 (2003) 368.

G. A. Carini *et al.* IEEE Nuclear Science Symposium, Conference Record Oct. 26 2007- Nov. 3 2007 (2) 1603.

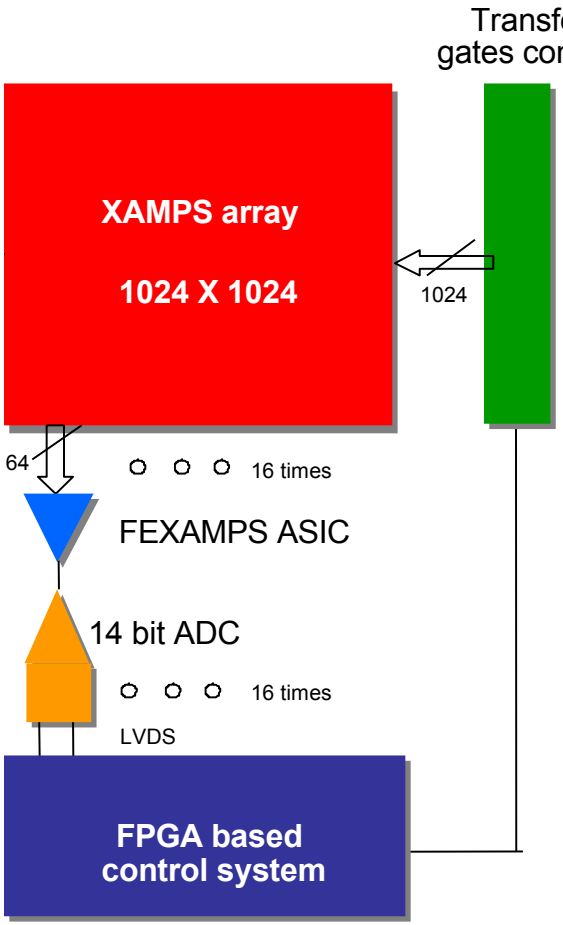
Active matrix

- Charge stored in diode capacitance
- Switches sequentially on, row by row
- Readout amplifiers in each column
- Charge readout and digitized
- Column to ADC multiplexing (each ADC readout 16 columns multiplexed)

~1 μs per row, ~1 ms for 1000 rows



System architecture



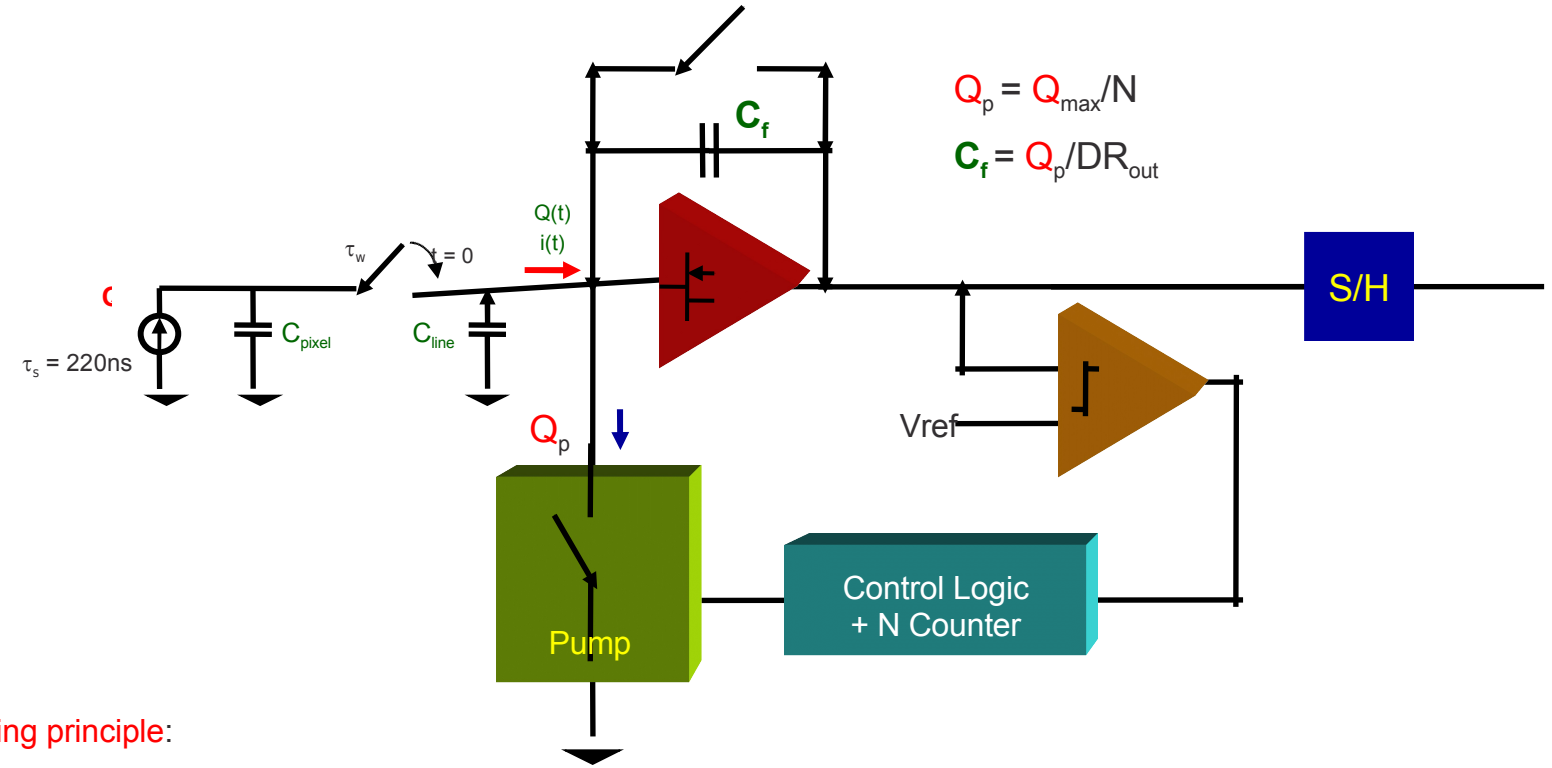
Front-end ASIC

- 64 front-end channels
- low-noise charge amplifier
- optimized time-variant filter
- Charge Pump
- dual Correlated Double Samplers
- 4 dual 16:1 multiplexers
- 4 Output buffers
- 20 MHz readout
- LVDS interface
- total 16 ASICs

Resolution (8 keV):	0.5 photons (FWHM)	500 e- rms
Dynamic range :	10^4 photons	2.2×10^7 e- (3.5 pC)
Pixel + line capacitance :	2-20 pF including the line (depend on the capacitive gate control) [15pF]	
Processing time :	< 8 µs (1 µs-8 µs to be synchronized with the beam period of 120Hz)	

Charge pump or 0 balance method

Problem is to handle both large signals and small signals while maintaining low noise for small signals. Circuit works by 'pumping' large charge packets out of integrator summing node until amplifier falls into linear operation, then digitizing remainder.

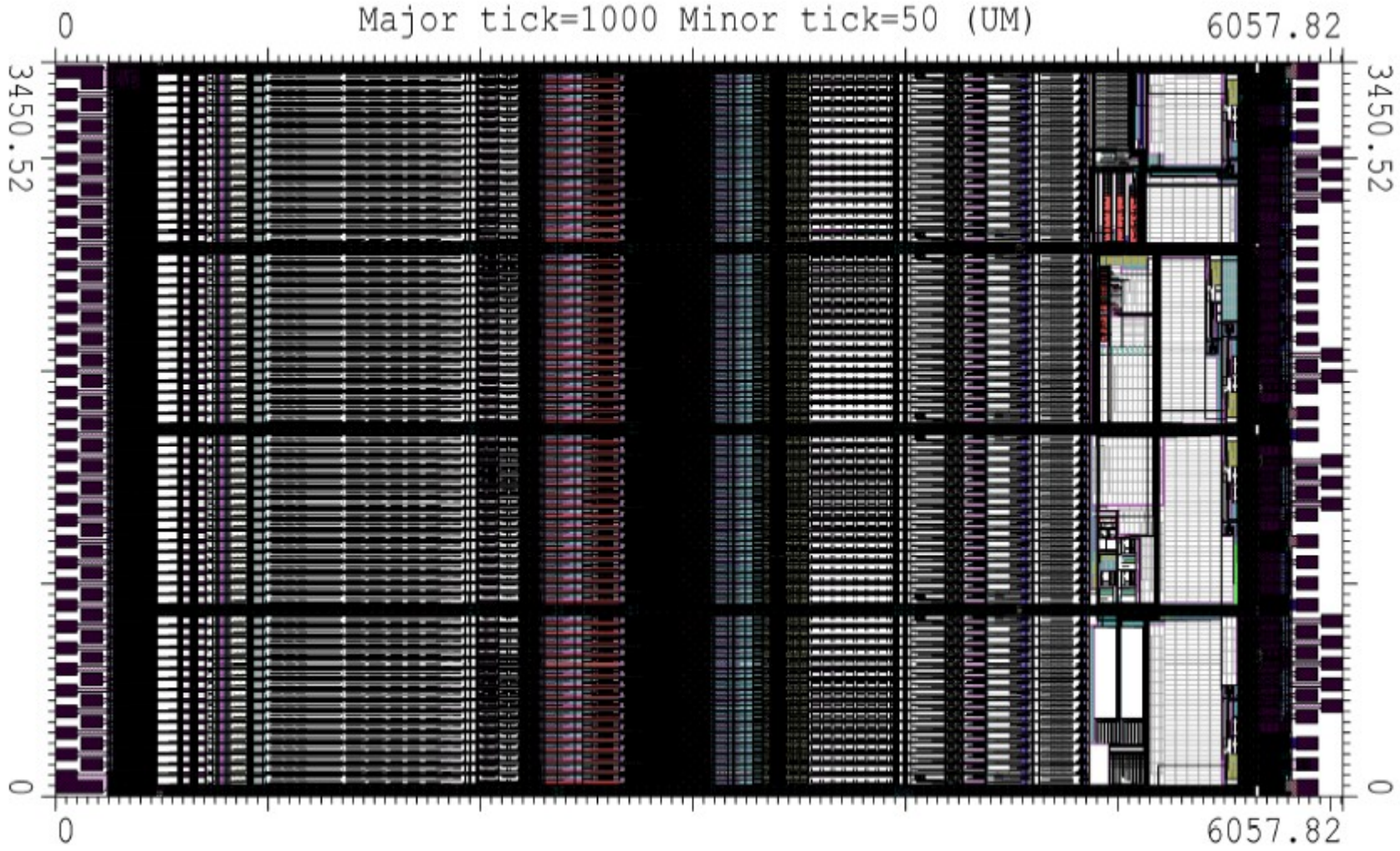


Working principle:

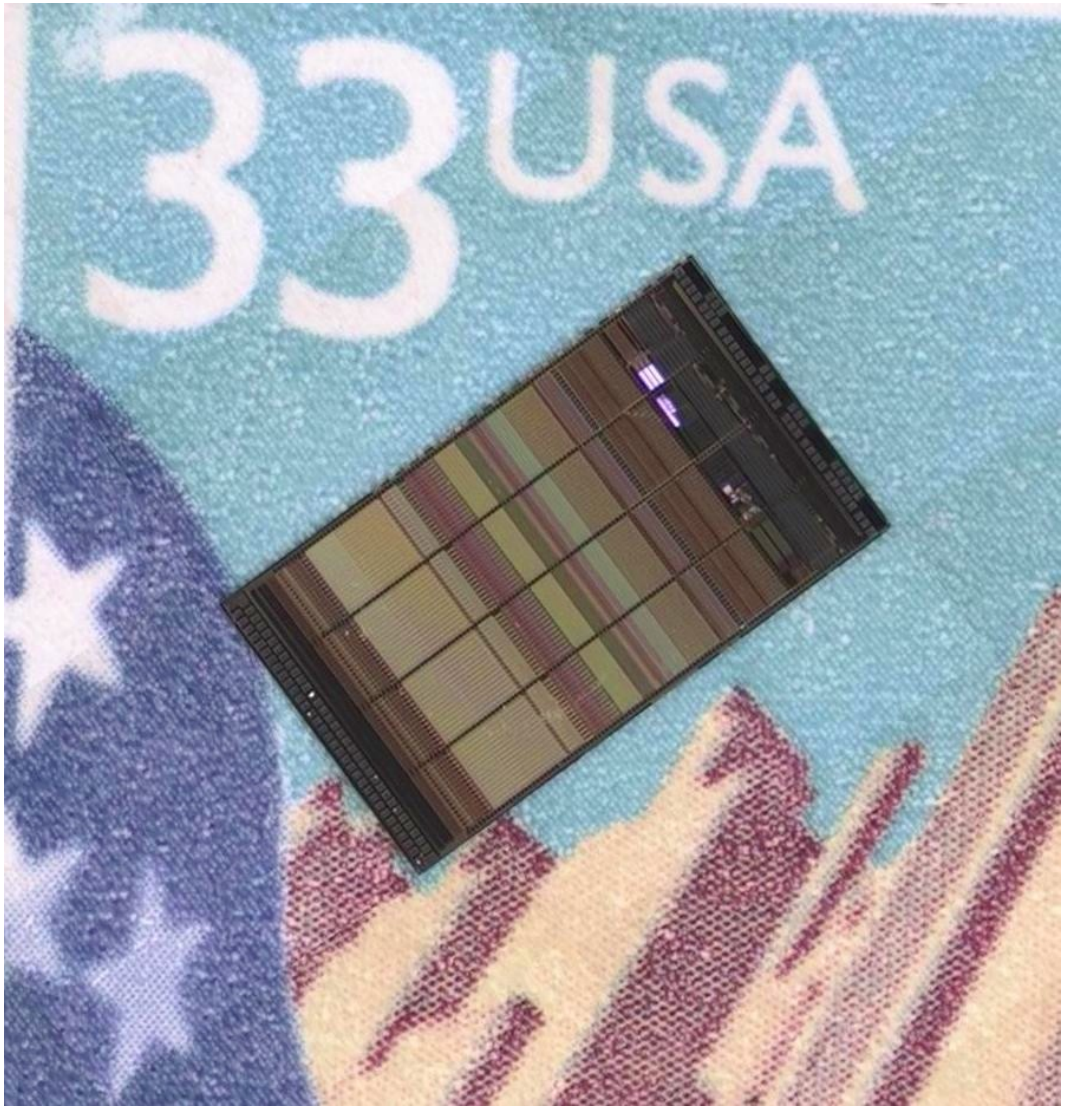
To meet the required resolution over the entire dynamic range a 0 balance method is applied: the dynamic range is divided in N ranges each one corresponding to a charge Qp=Qmax/N. When a charge larger than Qp is presented to the input a charge pump is activated to remove fixed amount of charge equal to Qp until a residual smaller than Qp remains stored in the feedback capacitor Cf. The number of charge quanta Qp removed by the pump are counted and the corresponding digital value is presented at the output representing the most significant bits of the final A/D conversion (for N=8 we have 3 bit).

The residual charge in the feedback capacitor is then sampled according to a CDS scheme, presented at the output and converted with a 14bit ADC (total of 14+3=17bit).

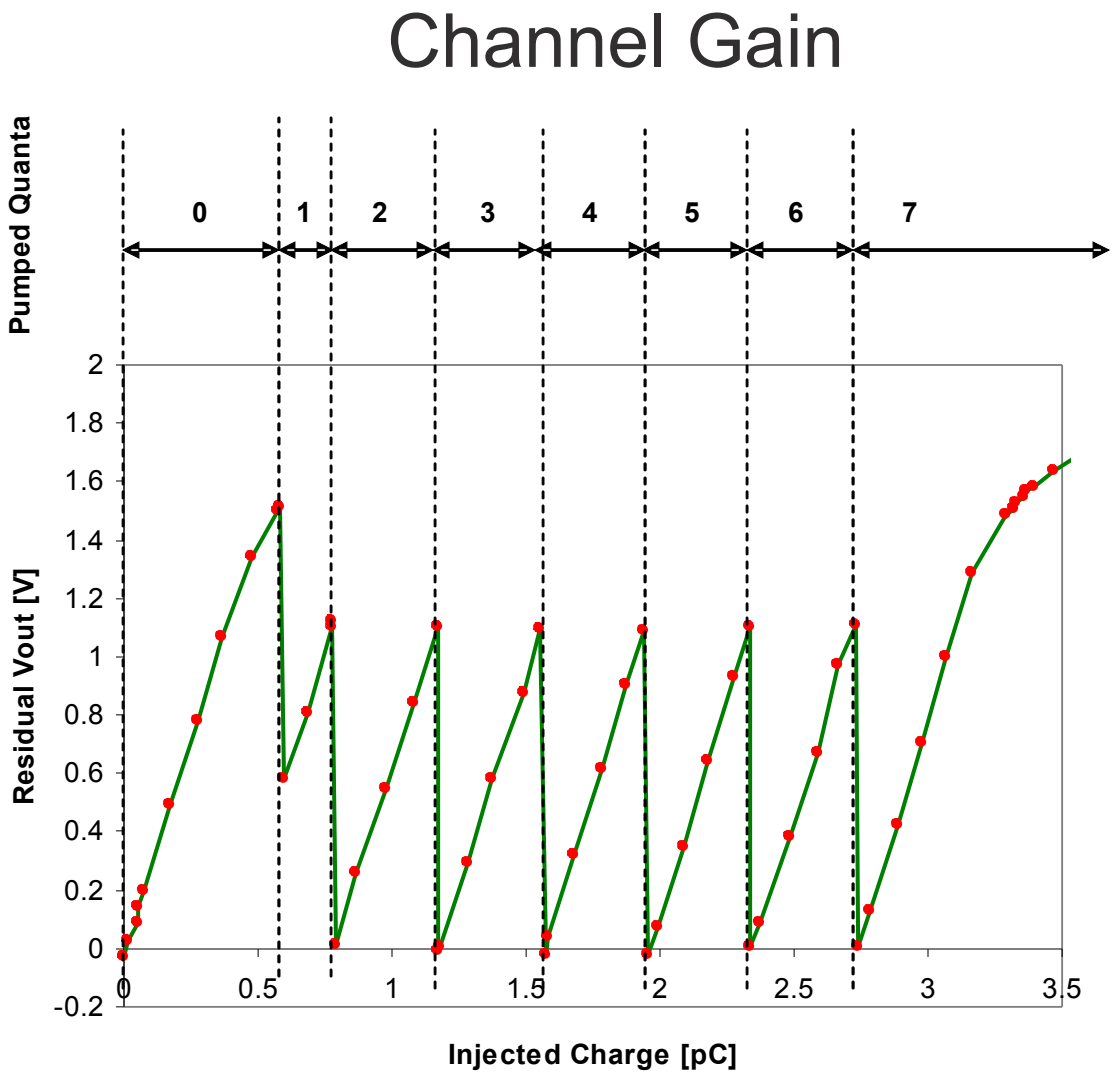
Final layout and chip size



Die cut



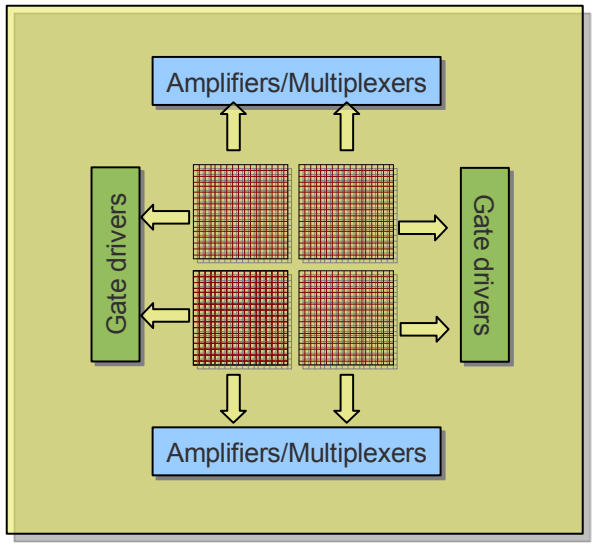
Preliminary results.



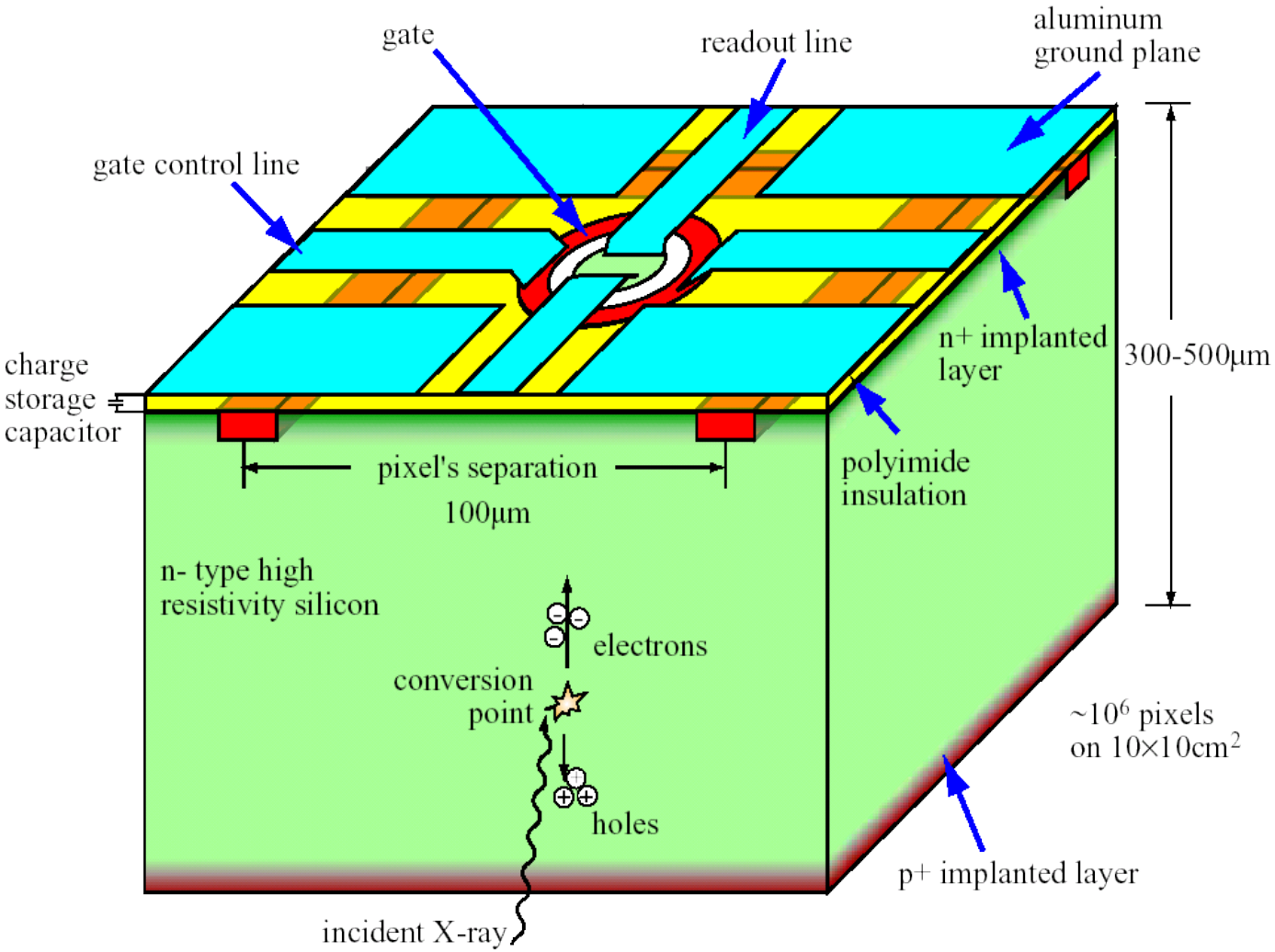
A. Dragone *et al.* (to be presented at IEEE Nuclear Science Symposium, 2008).

Sensors

- 512x512 pixels matrices tiled in 2x2 array:
  - in house fabrication
  - J-FET technology
  - 100 mm wafers
  - 400 µm thickness
  - 90 µm x 90 µm pixel size



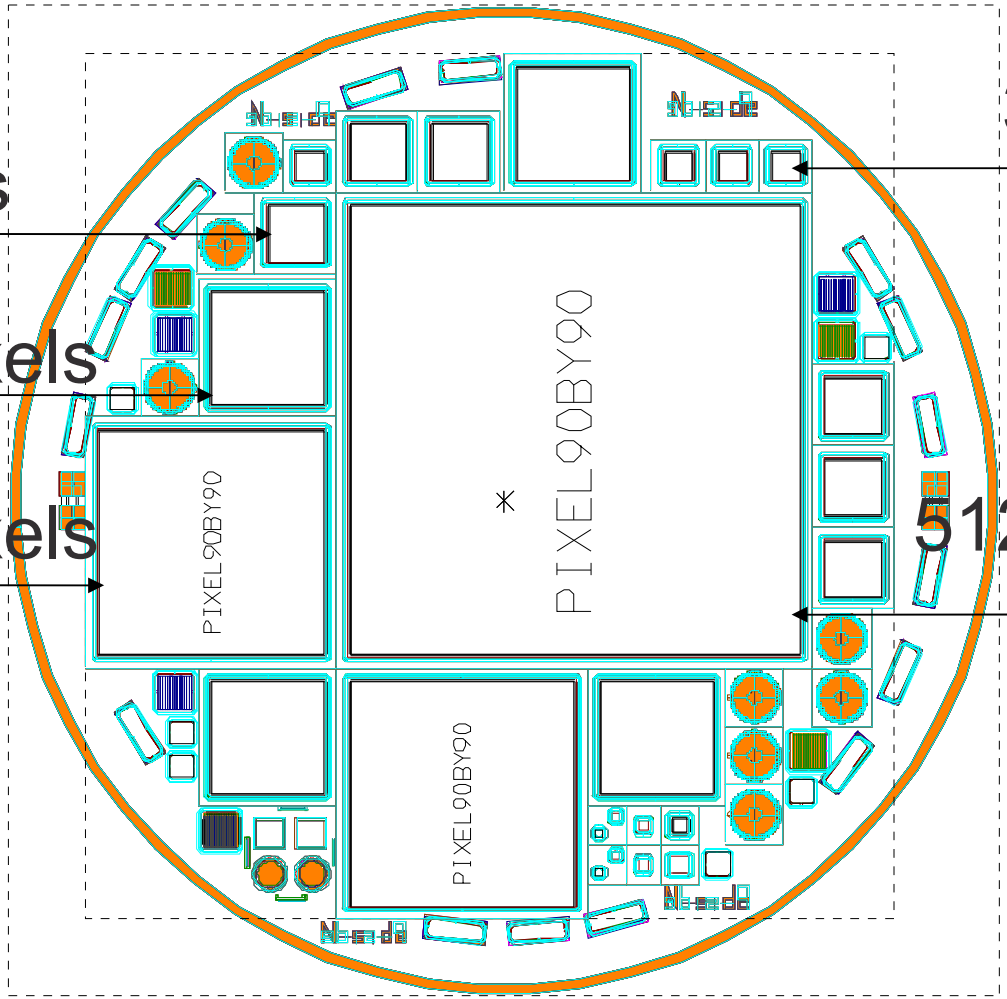
3D plot of a pixel



Fabrication

- Brookhaven's Instrumentation Division: Semiconductor Detector Development and Processing Lab (SDDPL).
  - 600 sq. ft. class-100 cleanroom
  - J-FET technology available on 100 and 150 mm wafers

Masks' Layout



64x64 pixels

128x128 pixels

256x256 pixels

32x32 pixels

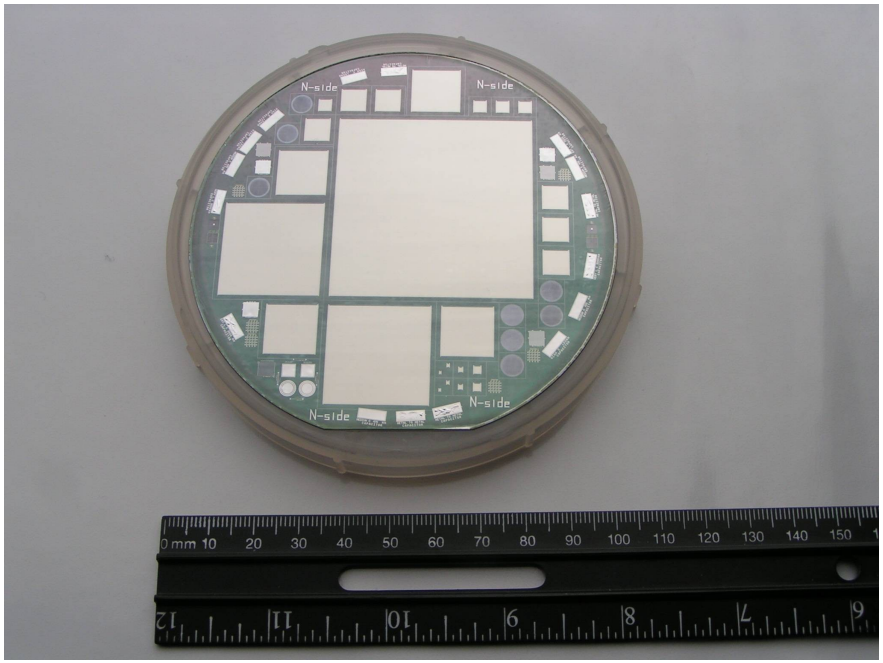
512x512 pixels

16x16 pixels, 8x8 pixels, 4x4 pixels, 2x2 pixels, and other test structures are designed.

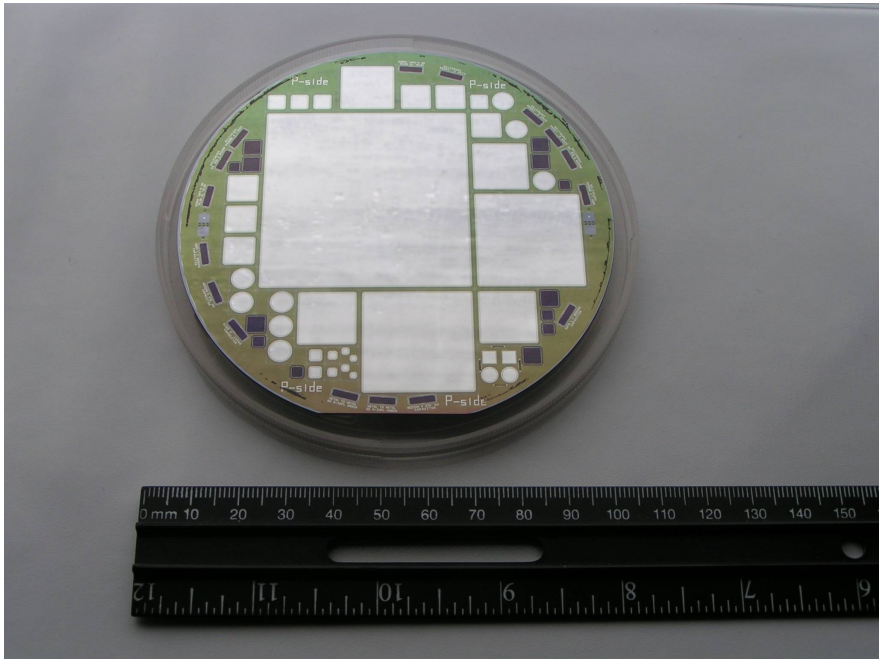
Detector processing steps

Mask Symbol	Full Description	Function **12 Masks (16 mask steps)**
PNIN	**P**, **N** Implant on **N**-side	open oxide for p and n implantations on N-side
PIMP	**P**, **IM**plant on **P**-side	open oxide for p implantation on P-side
NCVN	**N** be **C**o**V**ered on **N**-side	mask protecting n-region from p implantation on N-side
PCVN	**P** be **C**o**V**ered on **N**-side	mask protecting p-region from n implantation on N-side
PDPN	**P** **D**ee**P** implant on **N**-side	mask protecting rest area from deep p implant on N-side
NDPN	**N** **D**ee**P** implant on **N**-side	mask protecting rest area from deep n implant on N-side
NITN	**NIT**ride cut on **N**-side	oxide step cut to silicon for both n and p region on N-side
NITP	**NIT**ride cut on **P**-side	oxide step cut to silicon on P-side
ALUN	**ALU**minum on **N**-side	first layer of aluminum contact on N-side
ALUP	**ALU**minum on **P**-side	aluminum contact on P-side
POLN	**POL**yimide on **N**-side	make polyimide insulation layer on N-side
ALTN	**A**luminum on **T**op on **N**-side	second aluminum contact on N-side

Final Wafers



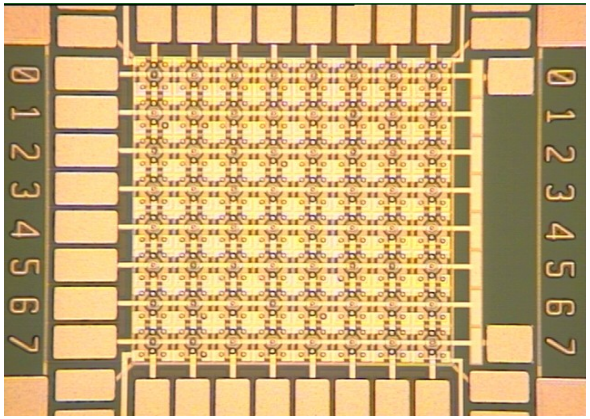
Device side



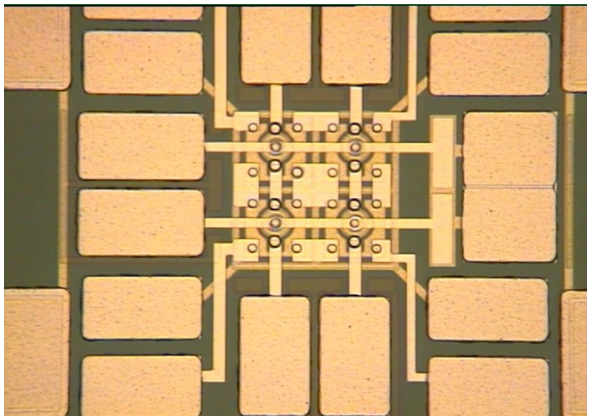
Window side

Some details

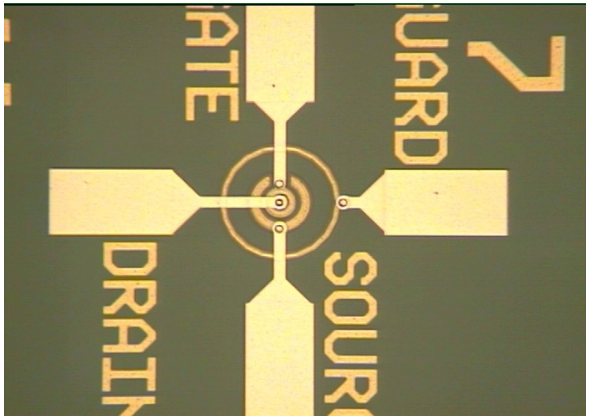
90 µm x 90 µm pixel size



matrix 8x8

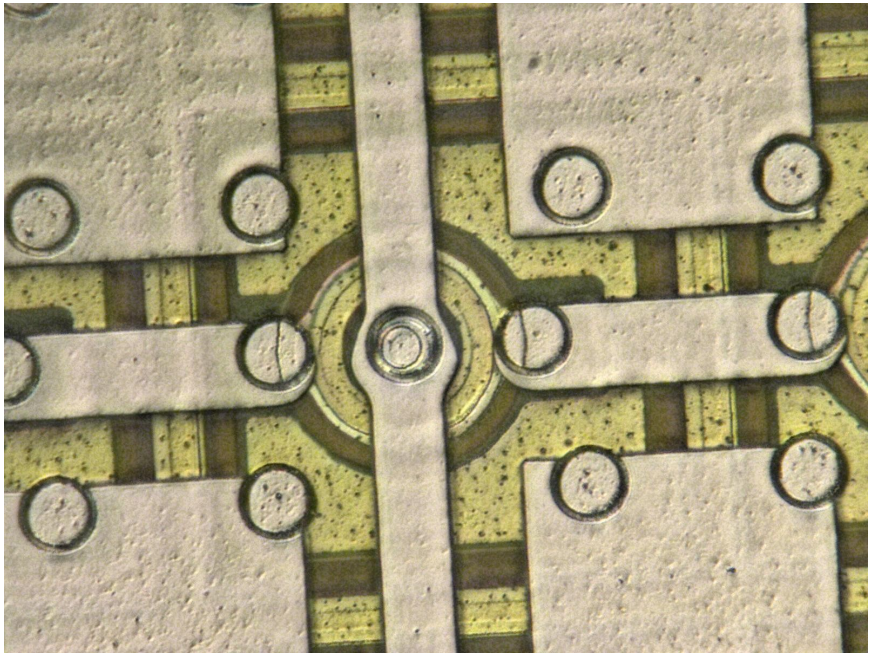


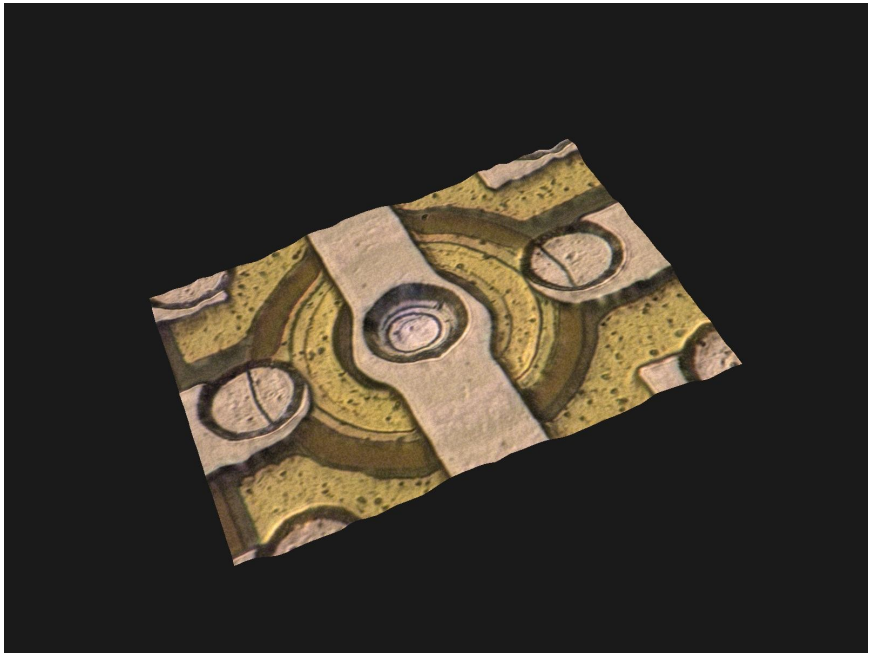
matrix 2x2



test transistor

Sensor details

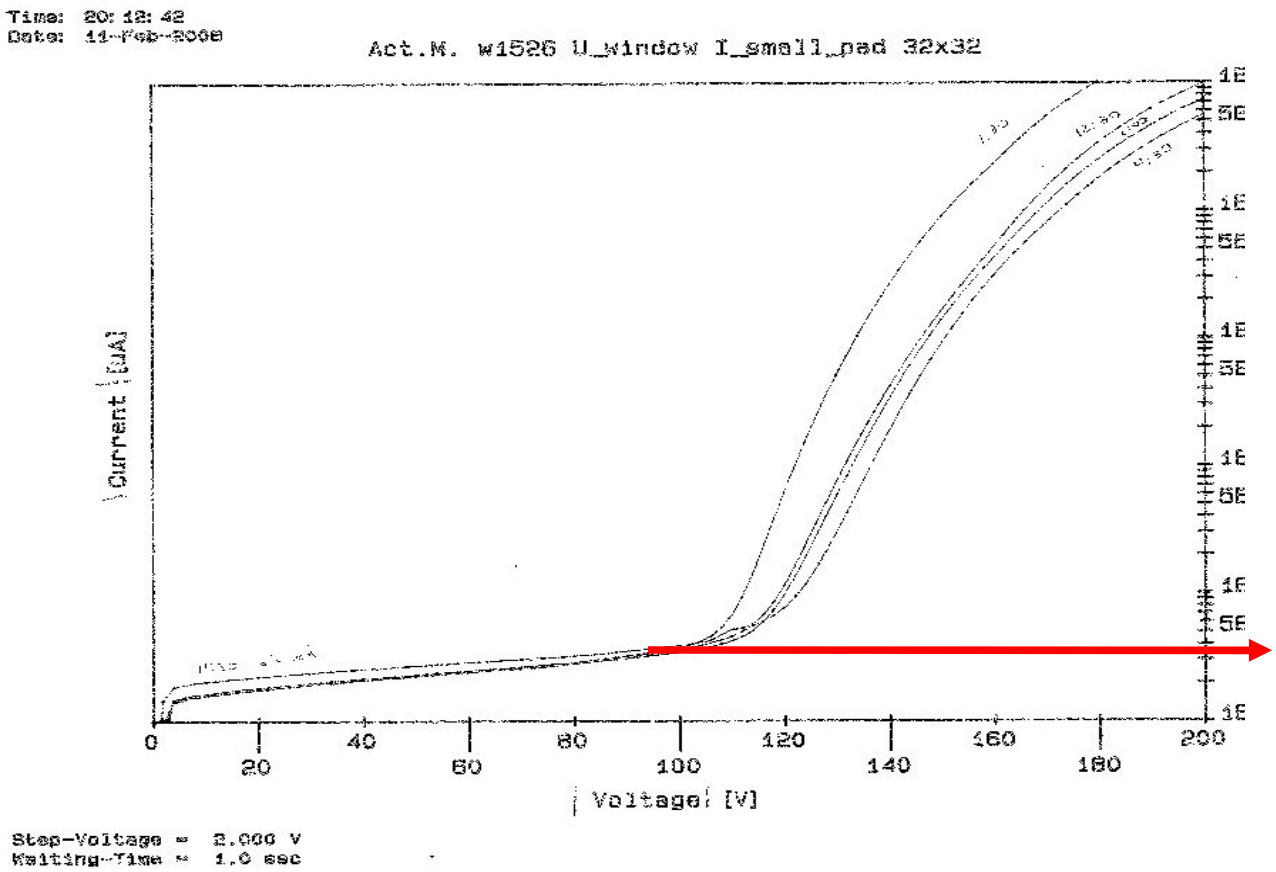




Pictures courtesy of Anand Kandasamy

Detail of a pixel: storage capacitor, gate and drain of the ring J-FET are visible with the pixels separator in the first metal. The second metal layer show part of a readout line (vertical line), switching line (two horizontal lines connected through vias to the gate), and planes connecting the capacitors where the charges are stored. The metal interlayer is a polyimide film.

I-V measurements

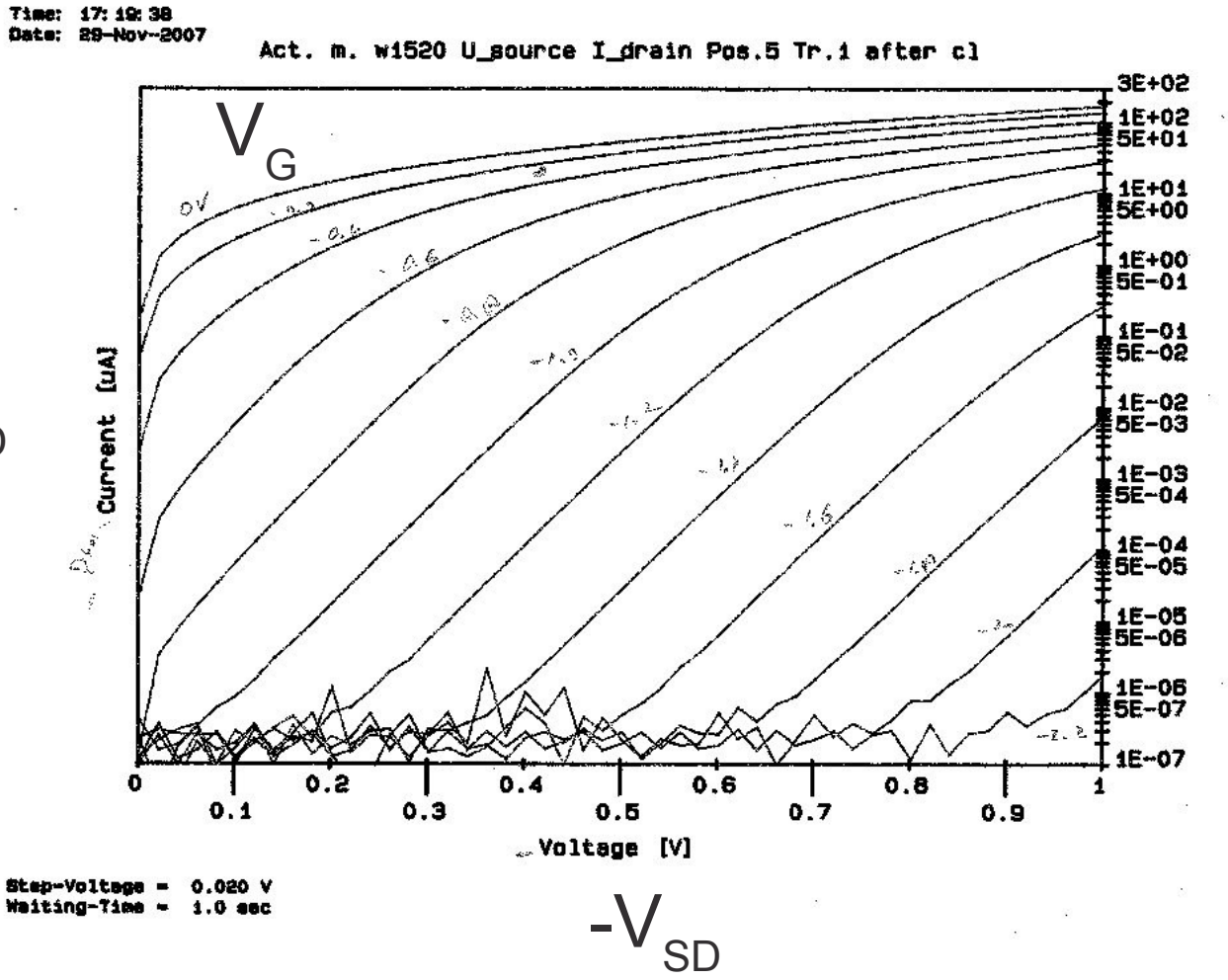


~300 pA
for 1024 pixels

~300 fA
per pixel

Dark current: 3.5 pA/cm^2
Room Temperature operation!

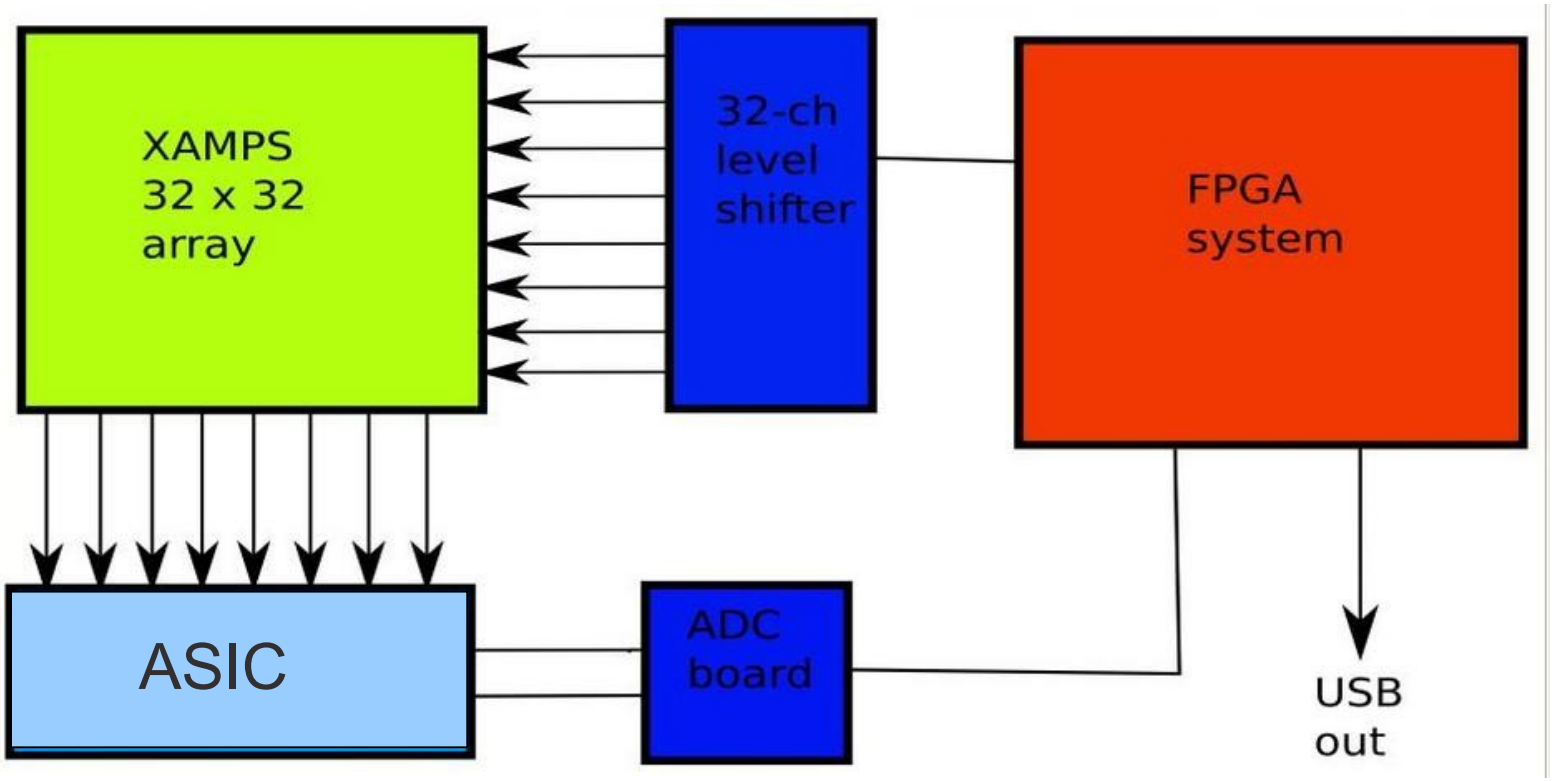
Transistor characteristics



$-I_D$

$-V_{SD}$

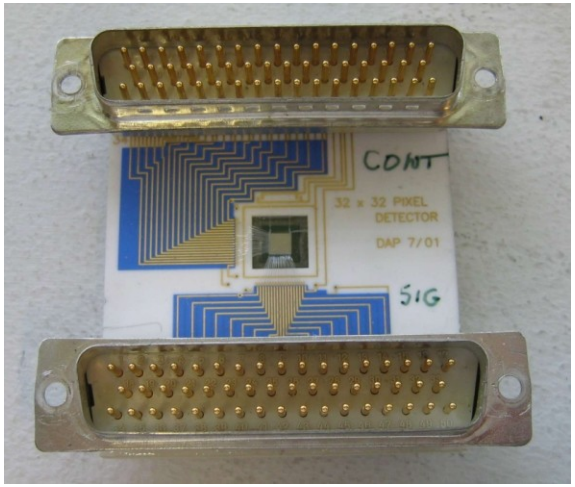
DAQ-1

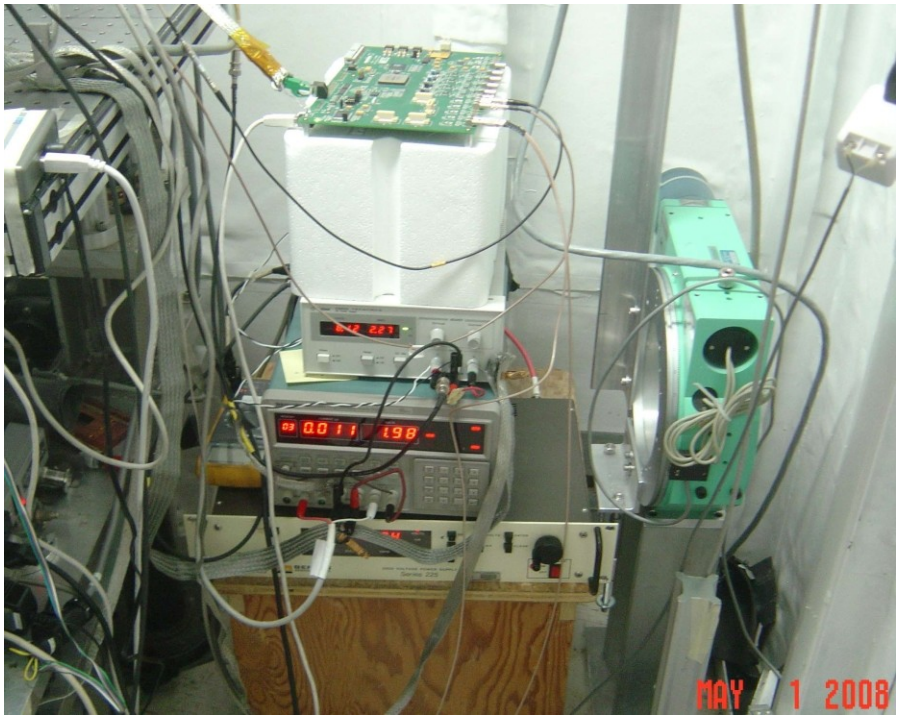


32 channel ASIC* front-end: low-noise charge preamplifier, shaper with stabilized baseline, discriminator and peak detector with an analog memory per channel. Readout sparsified.

*De Geronimo *et al*., Nuclear Science Symposium Conference Record, 2007. NSS '07. IEEE Volume 3, Oct. 26 2007-Nov. 3 2007 Page(s):2411 - 2415

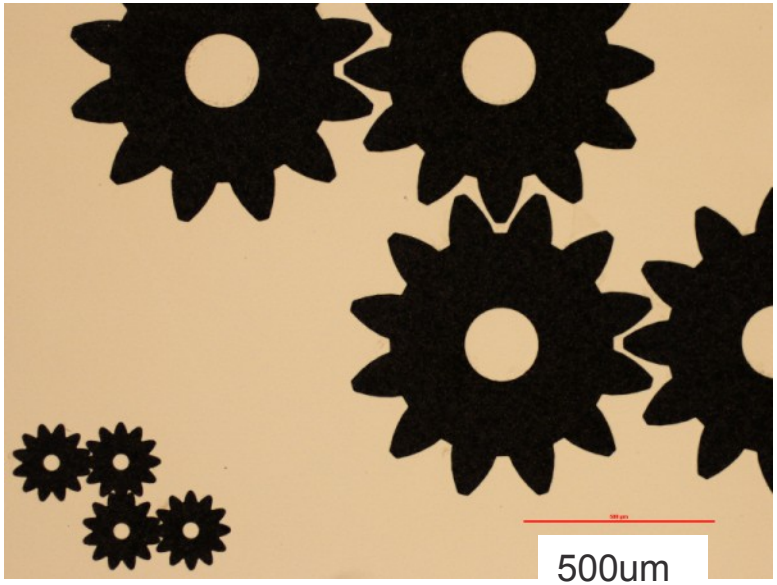
Setup

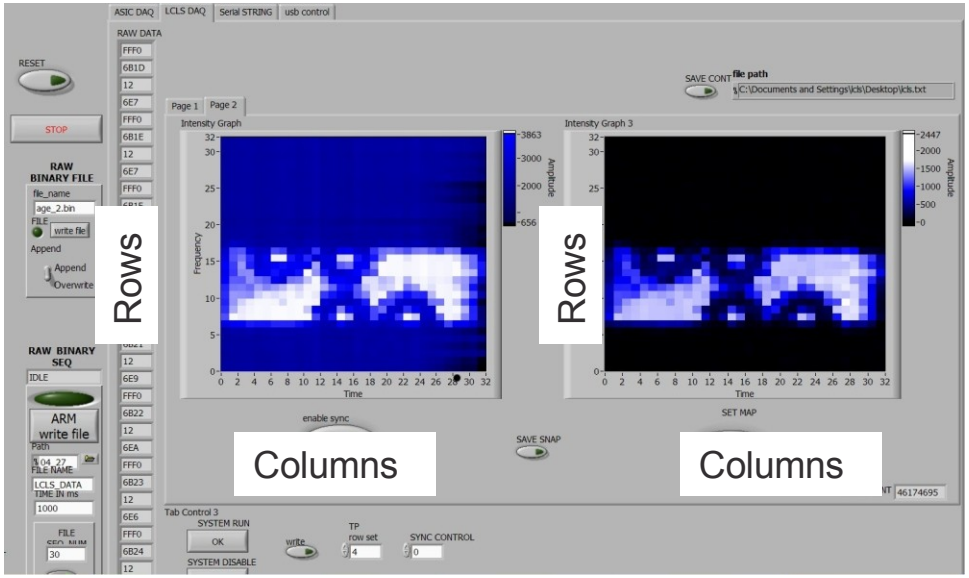




X12A – 8 keV

Quick Image

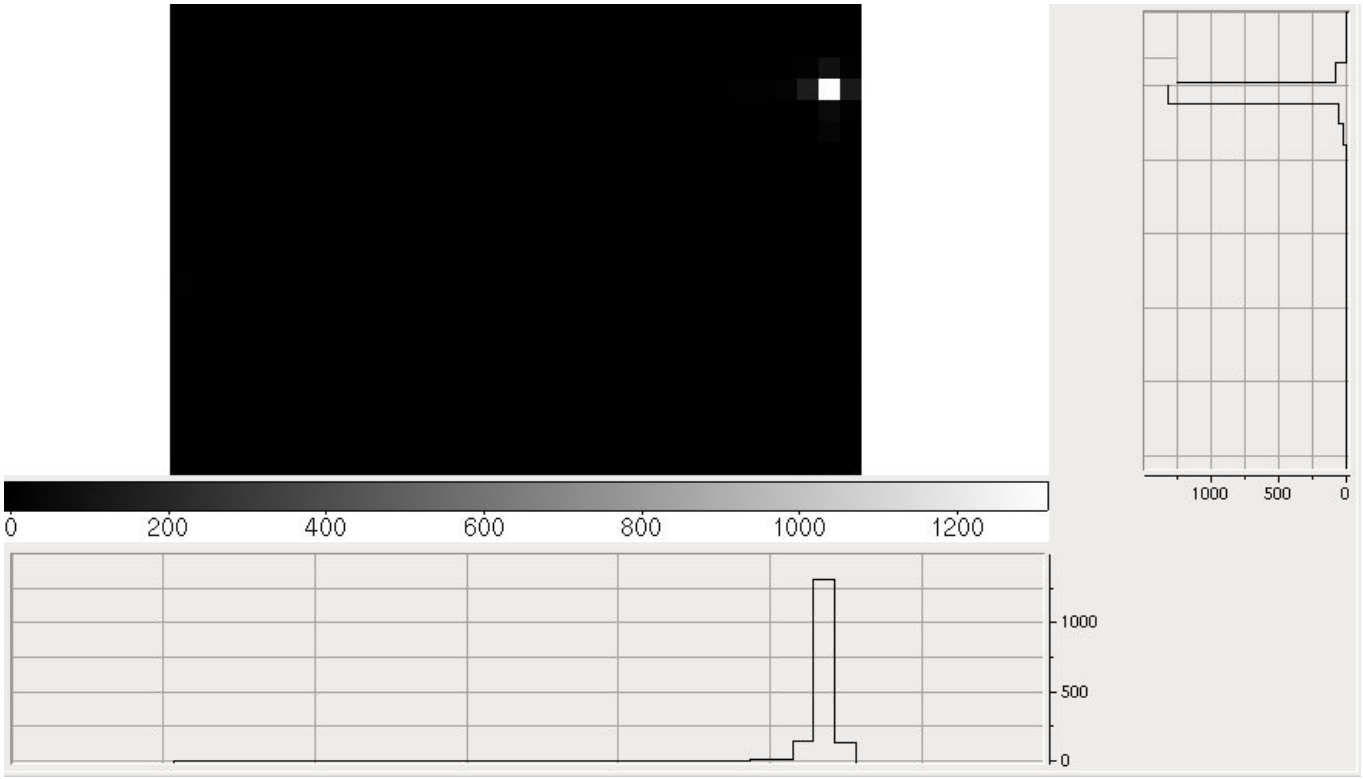




a) b)

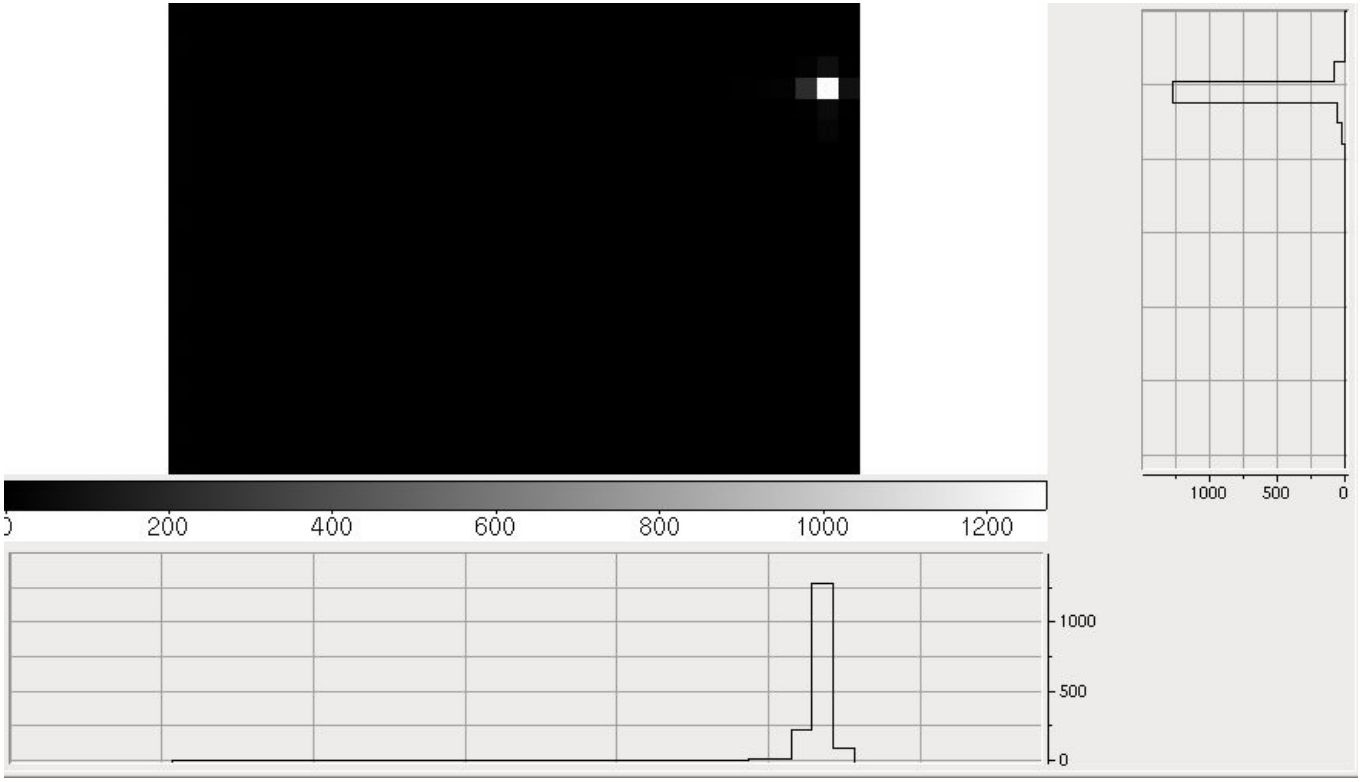
a) Detail of the lead mask. b) X-ray transmission image at 8 keV with a beam size of ~ 1 mm x 3 mm (VxH) and 8 ms integration time (left: raw data; right: background subtraction).

Raster scans



Scan performed with a monochromatic beam of 8 keV, 30 x 30 μm^2 beam size and with 10 μm step.

Raster scans



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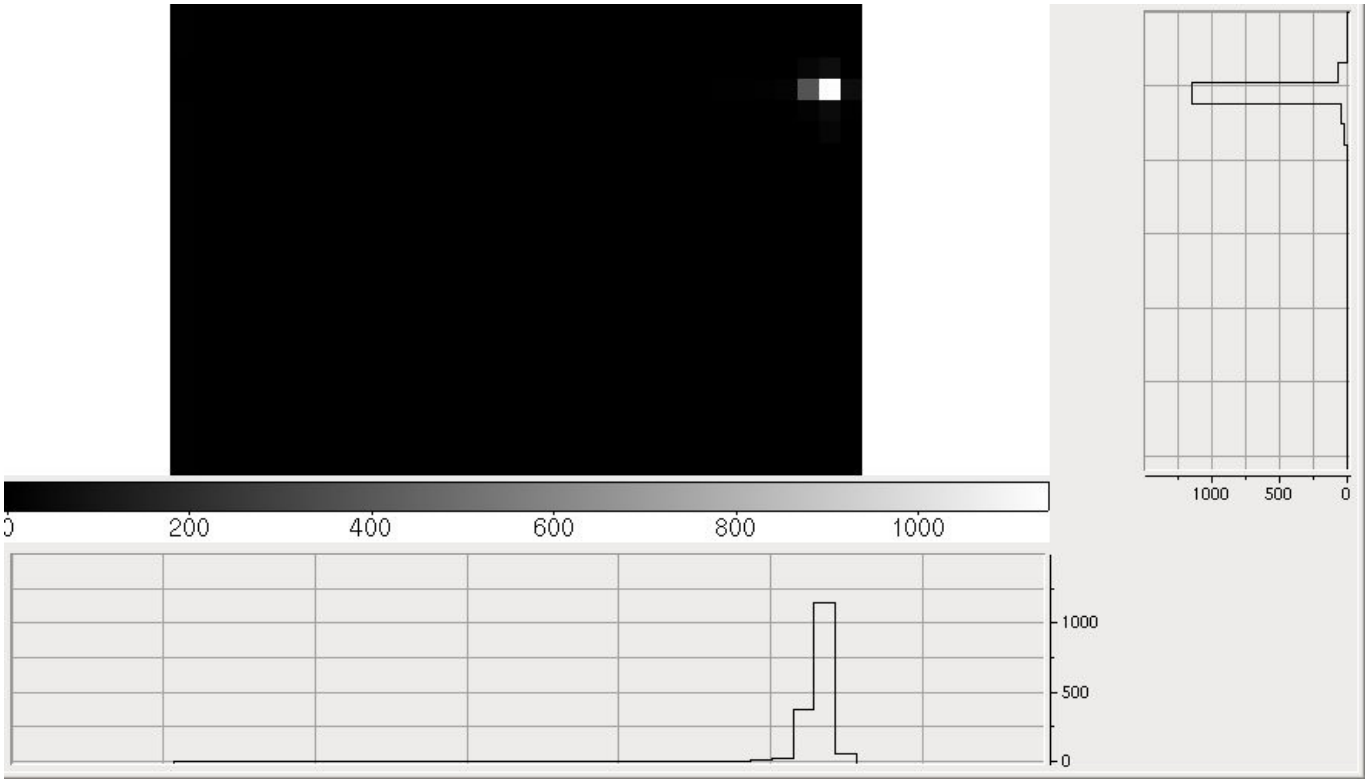

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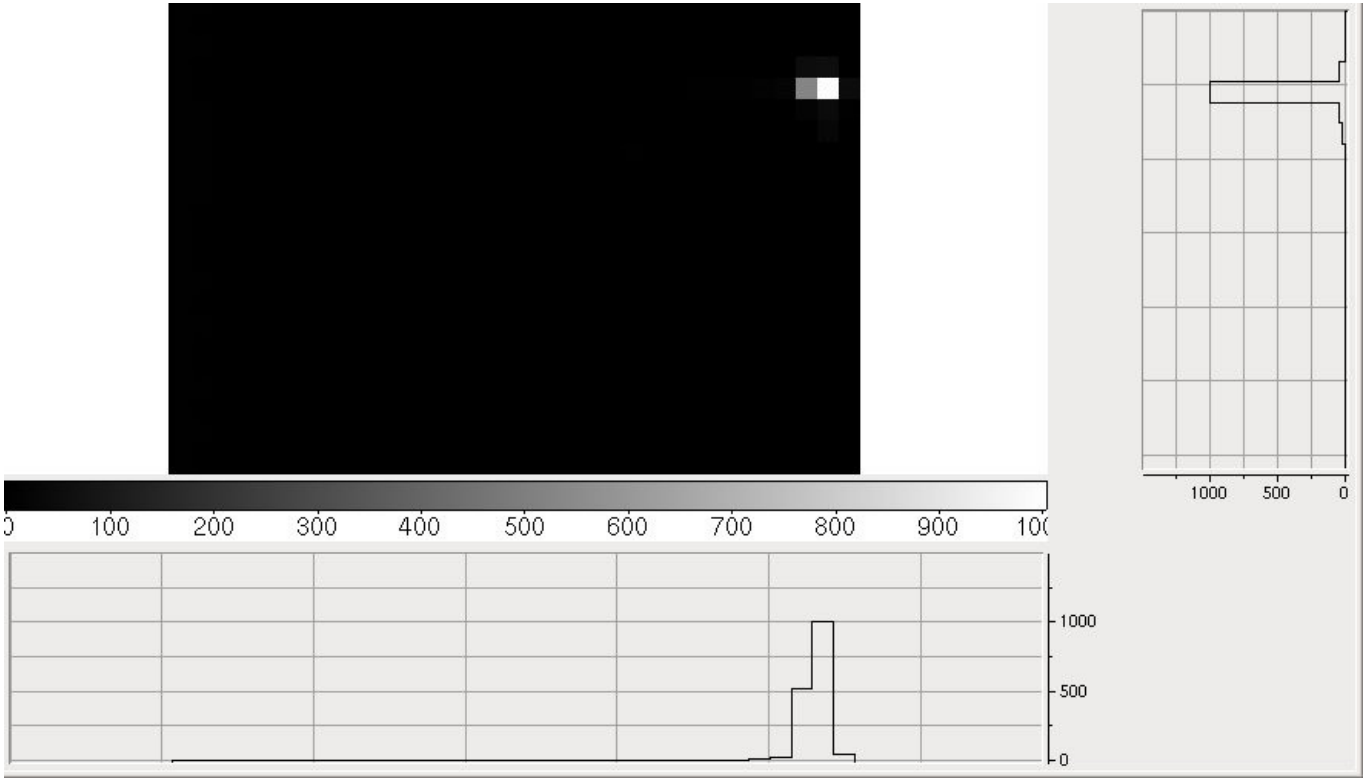

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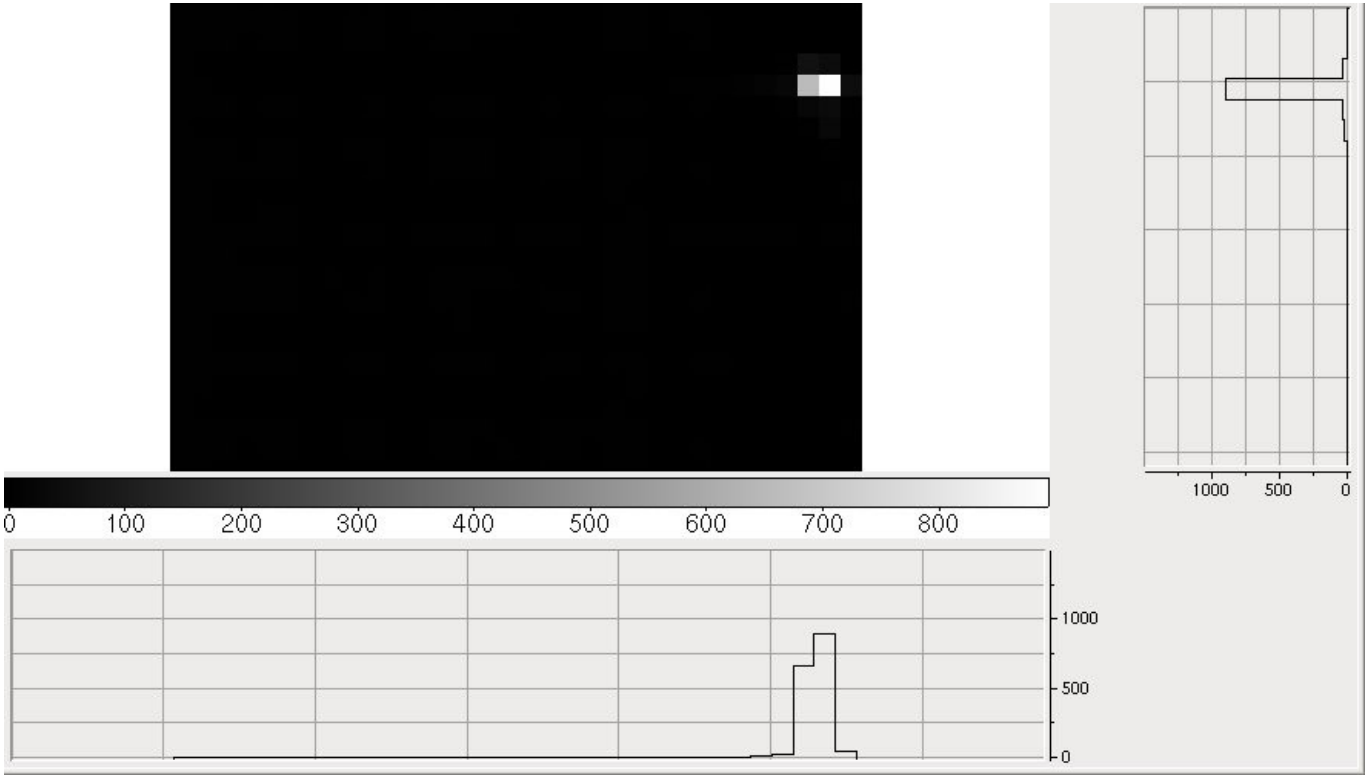

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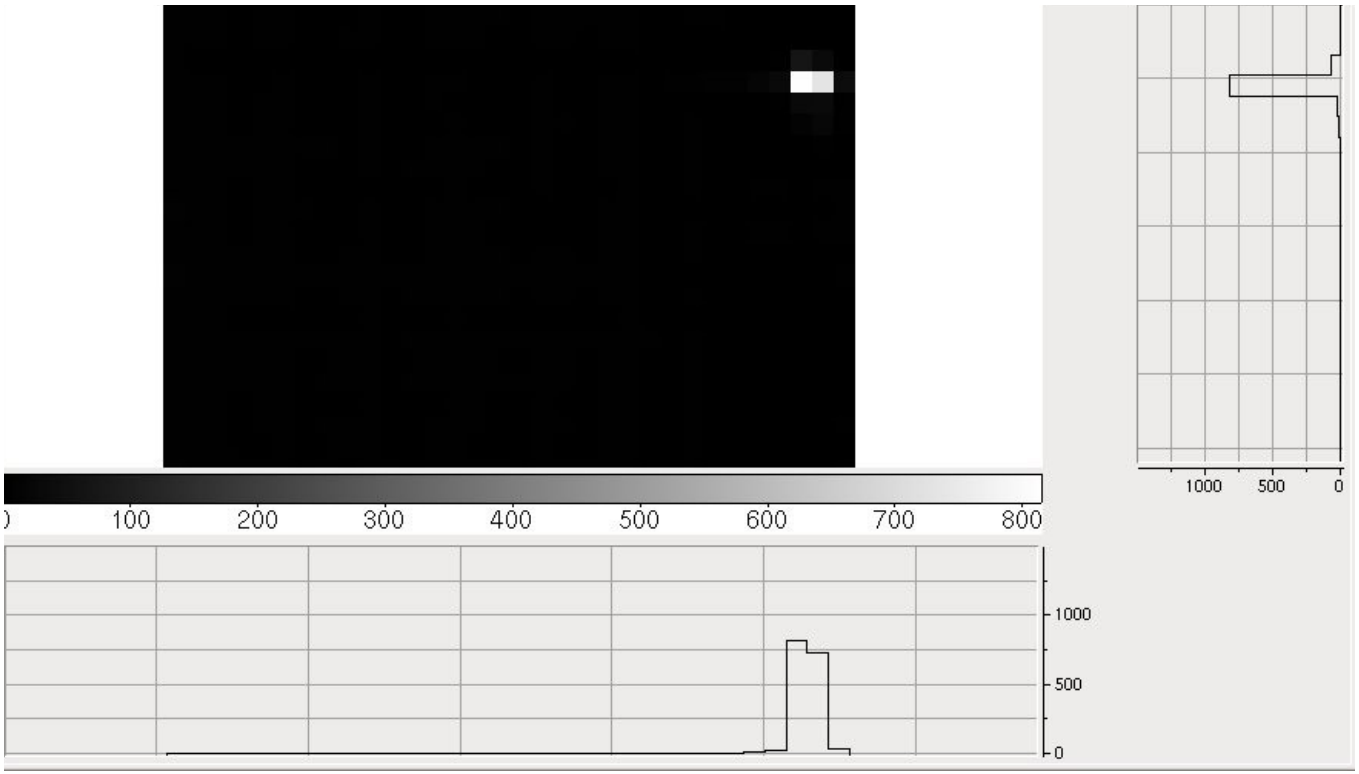

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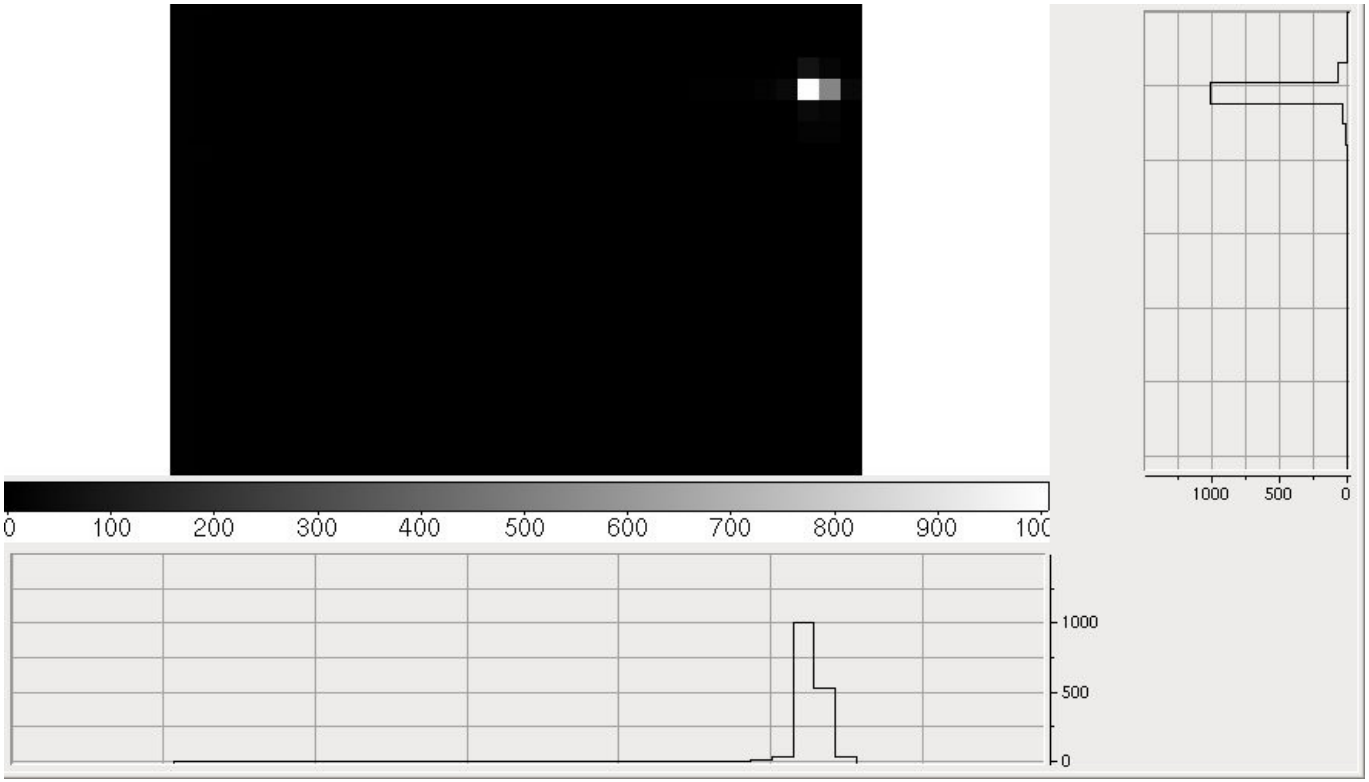

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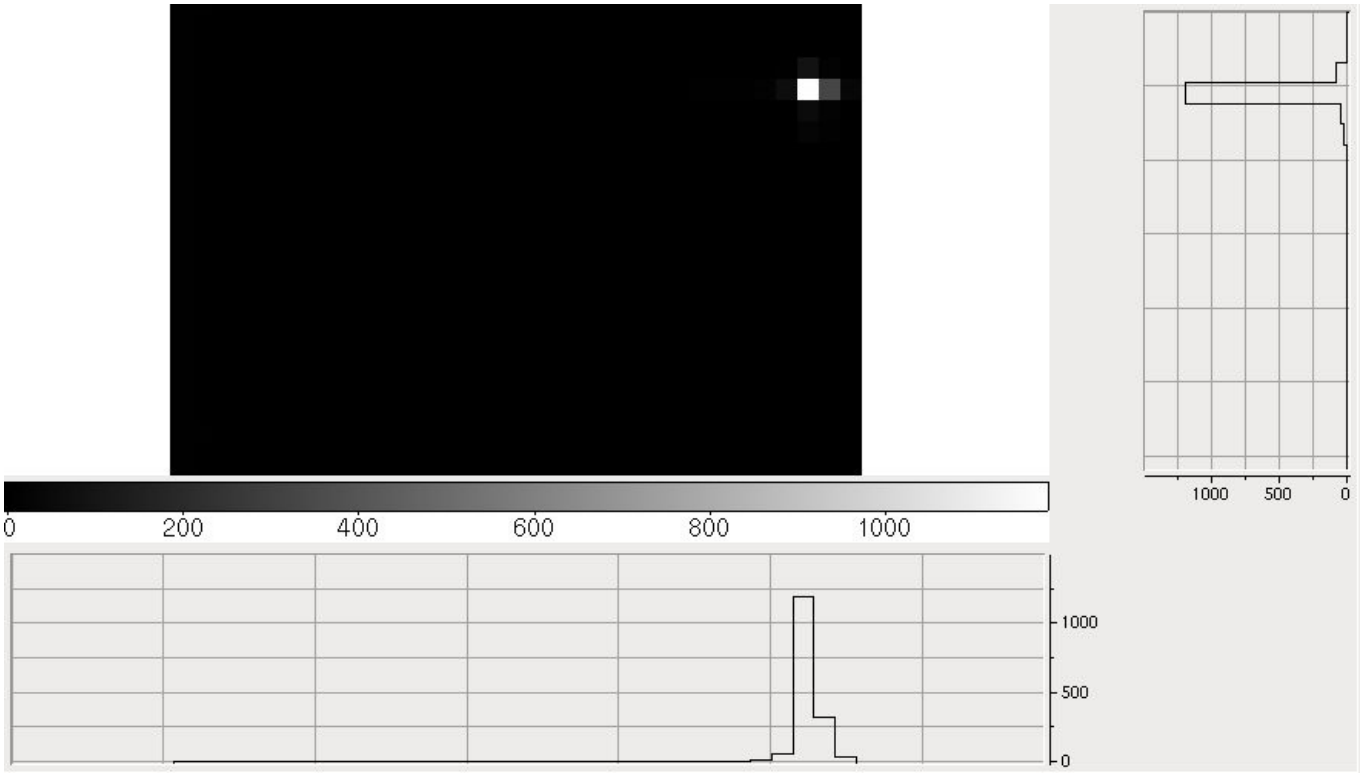
Raster scans



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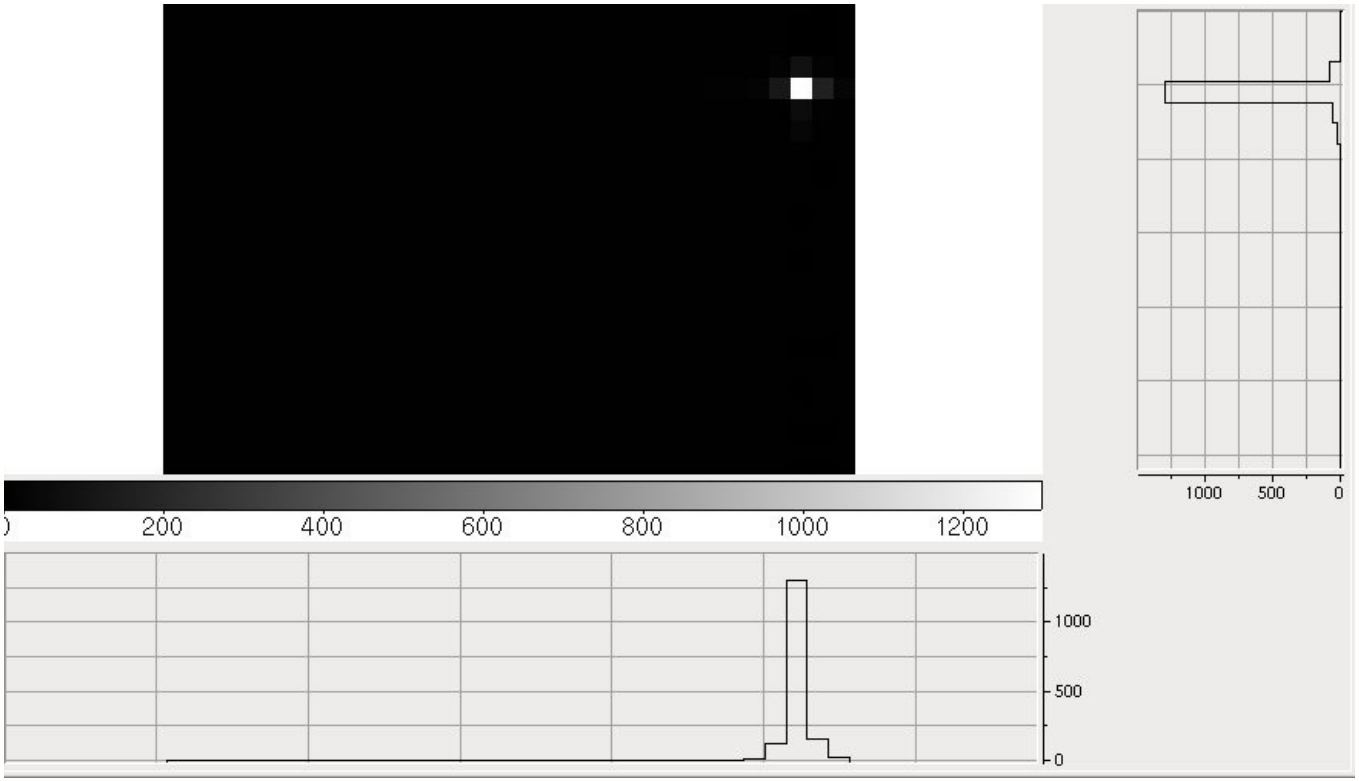

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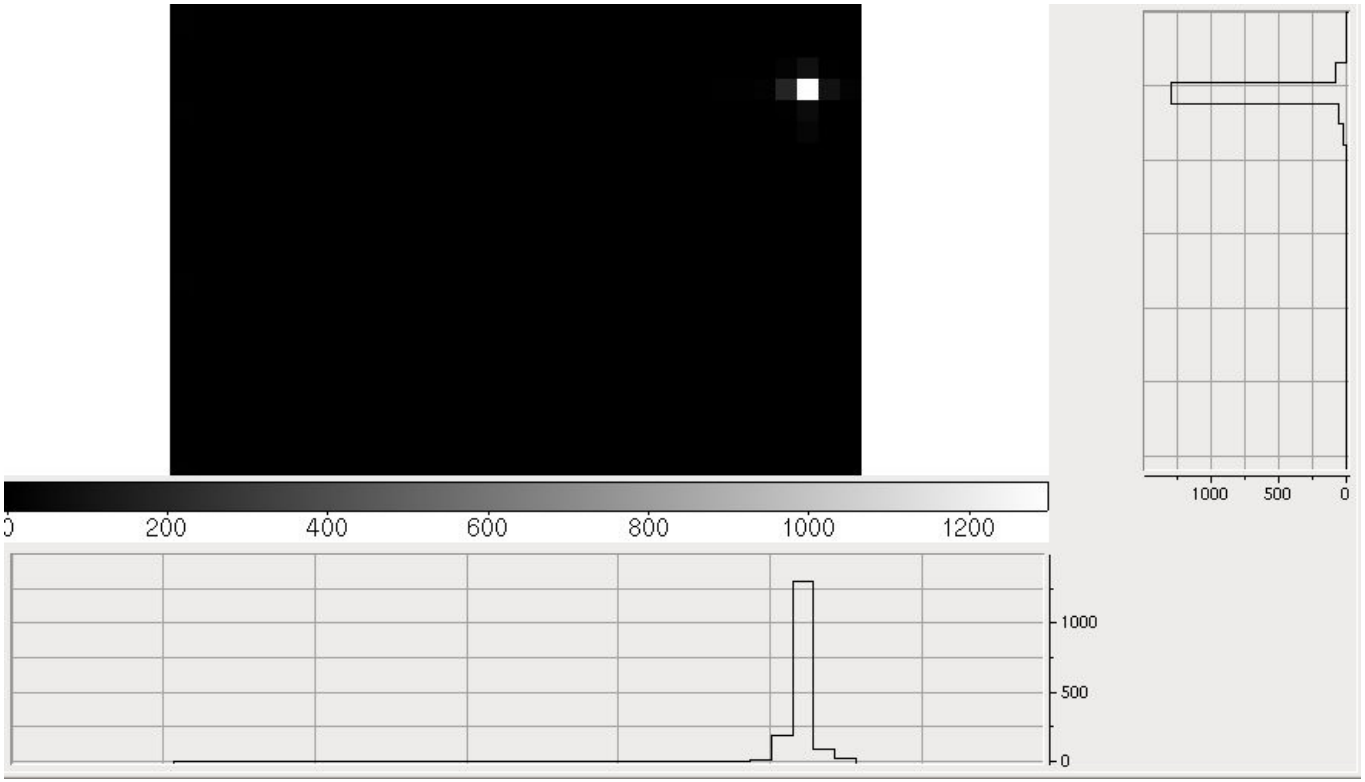

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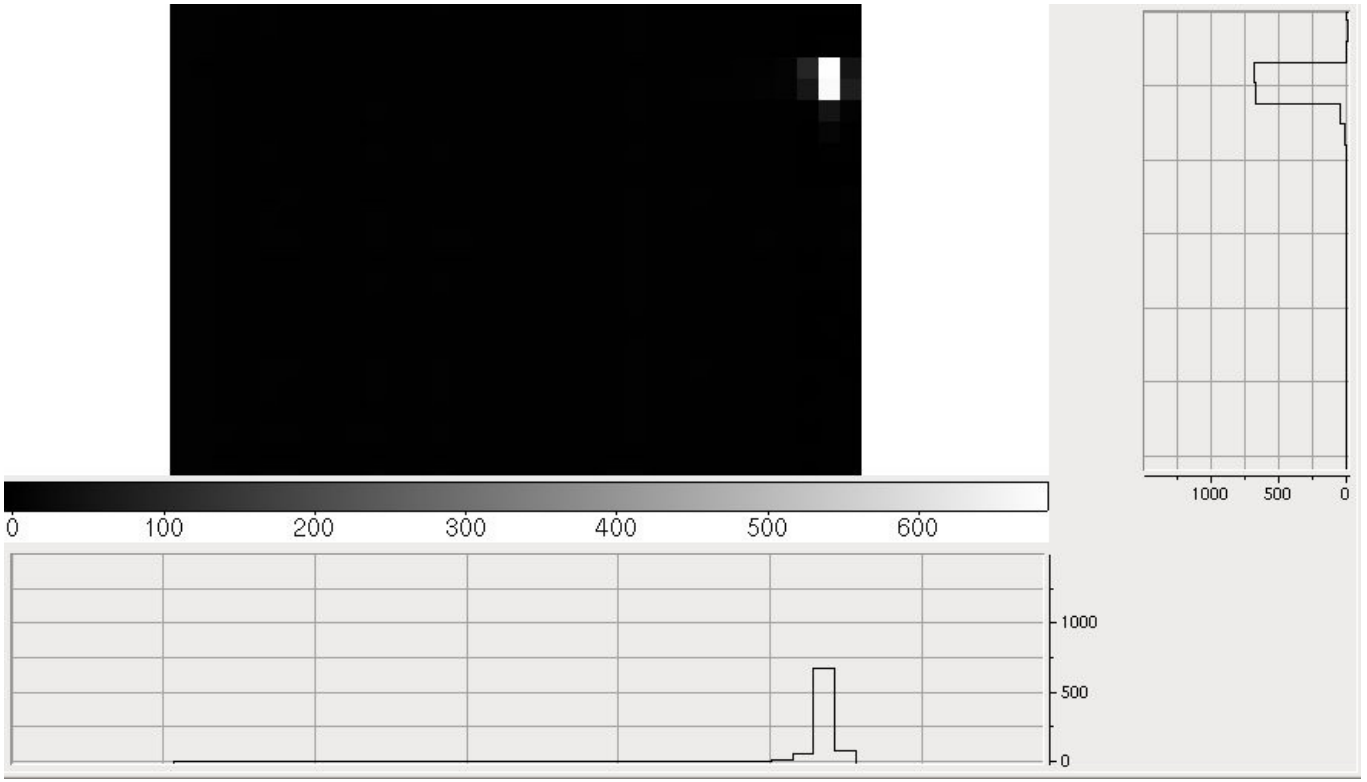

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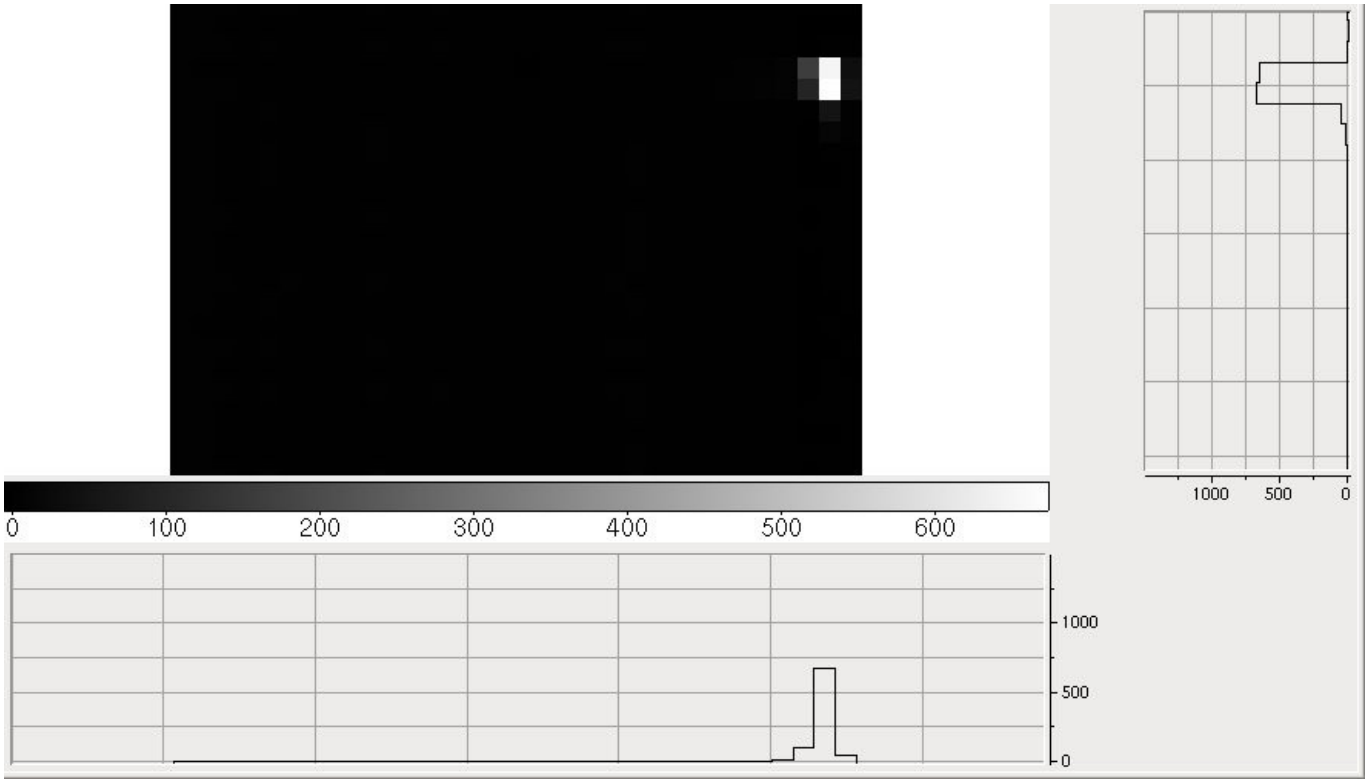

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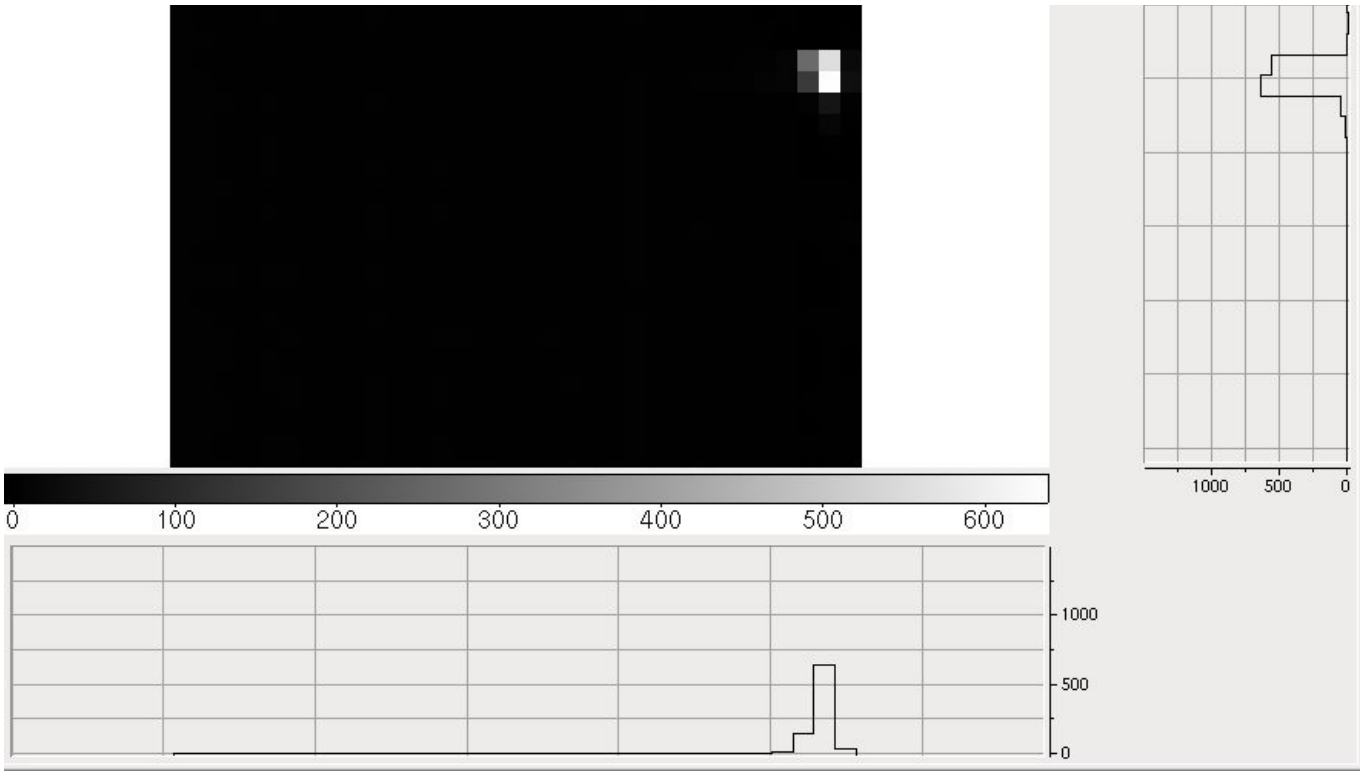

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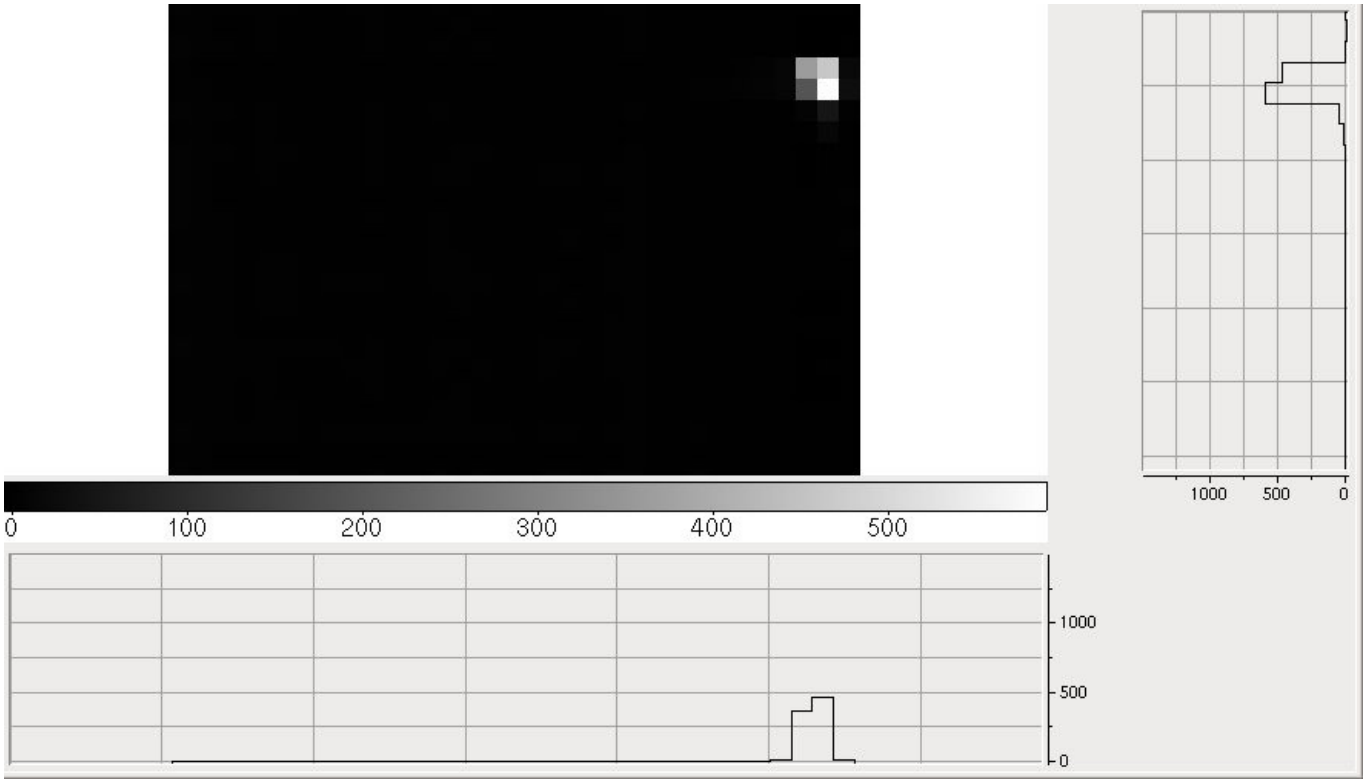

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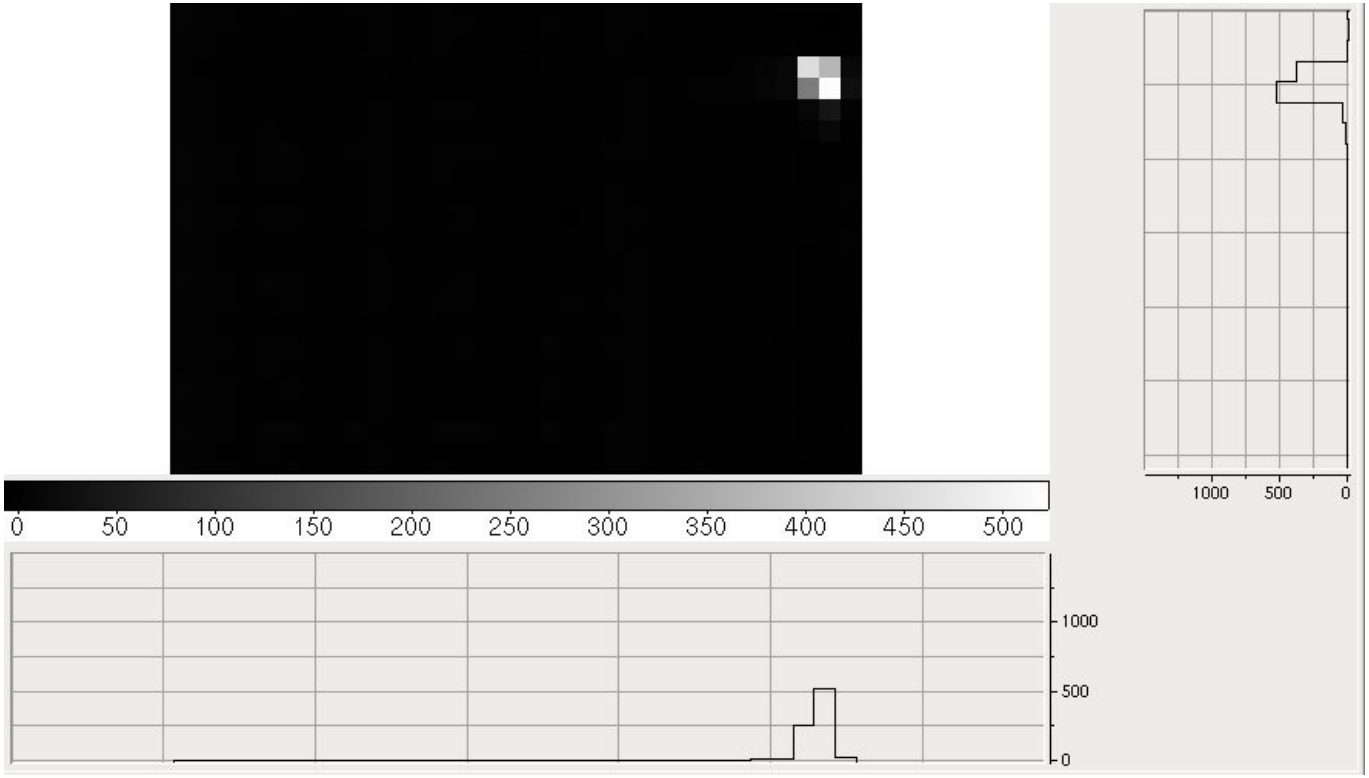

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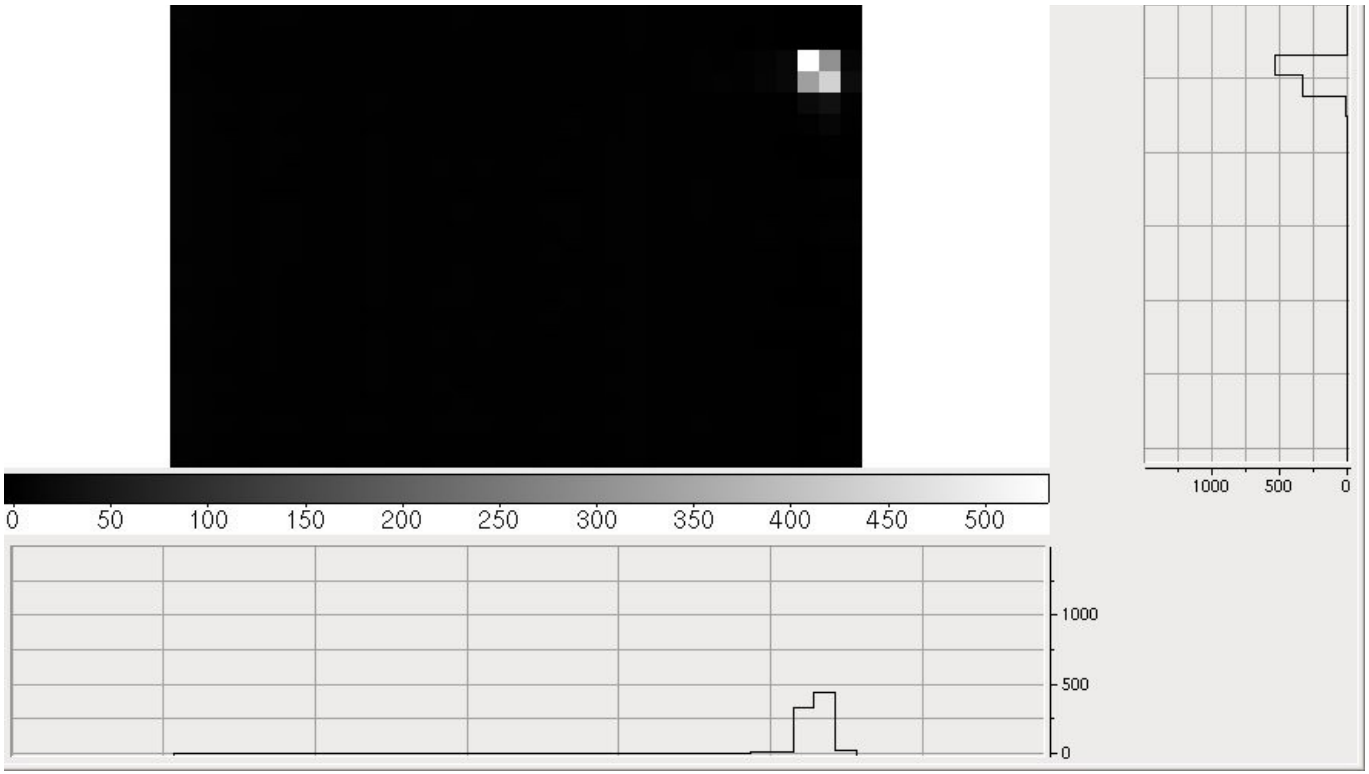

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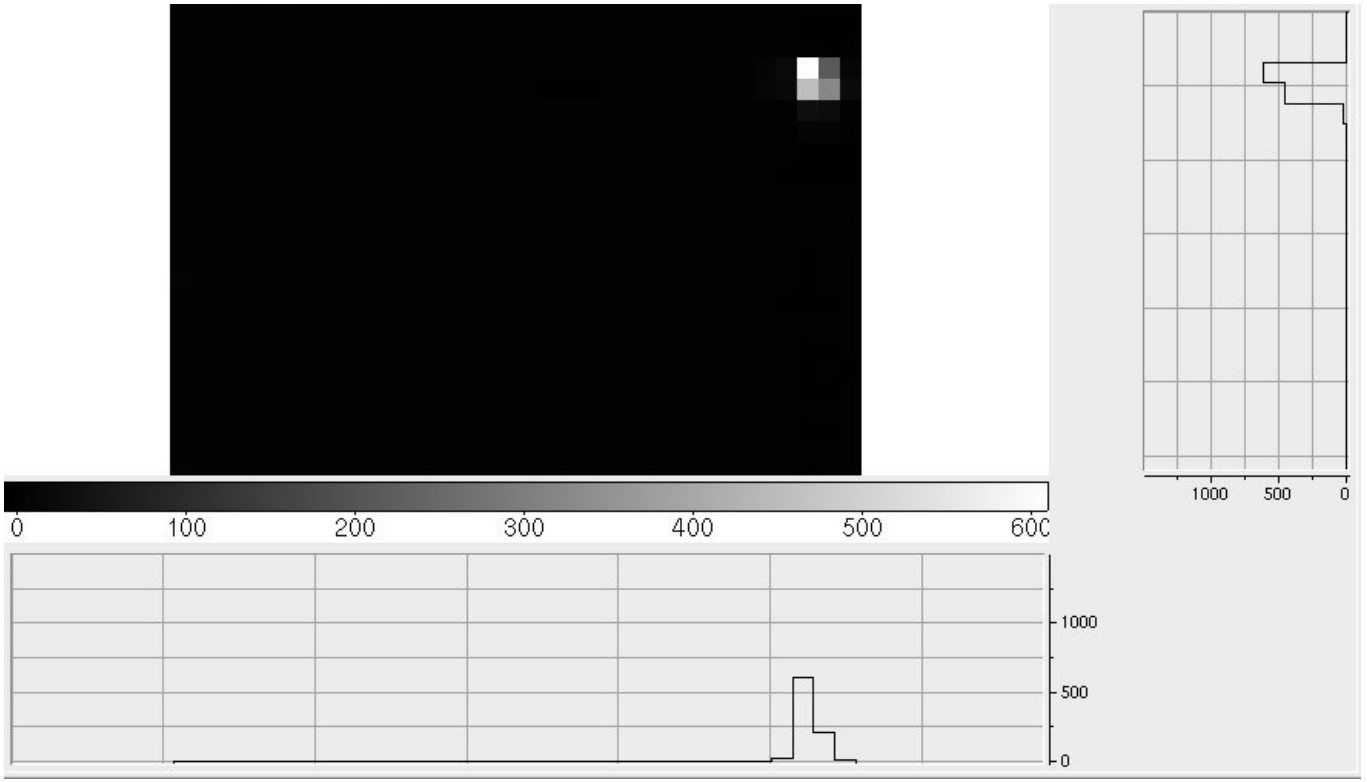
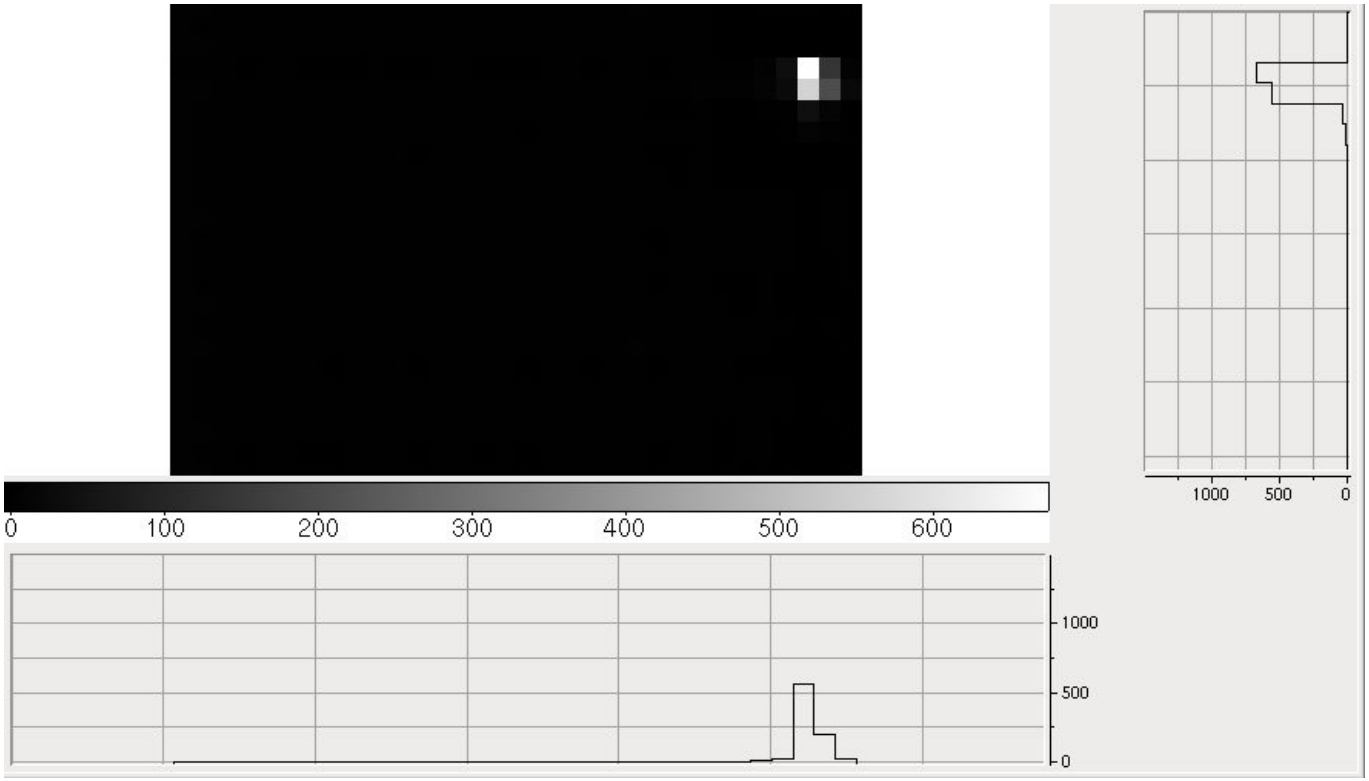
Raster scans



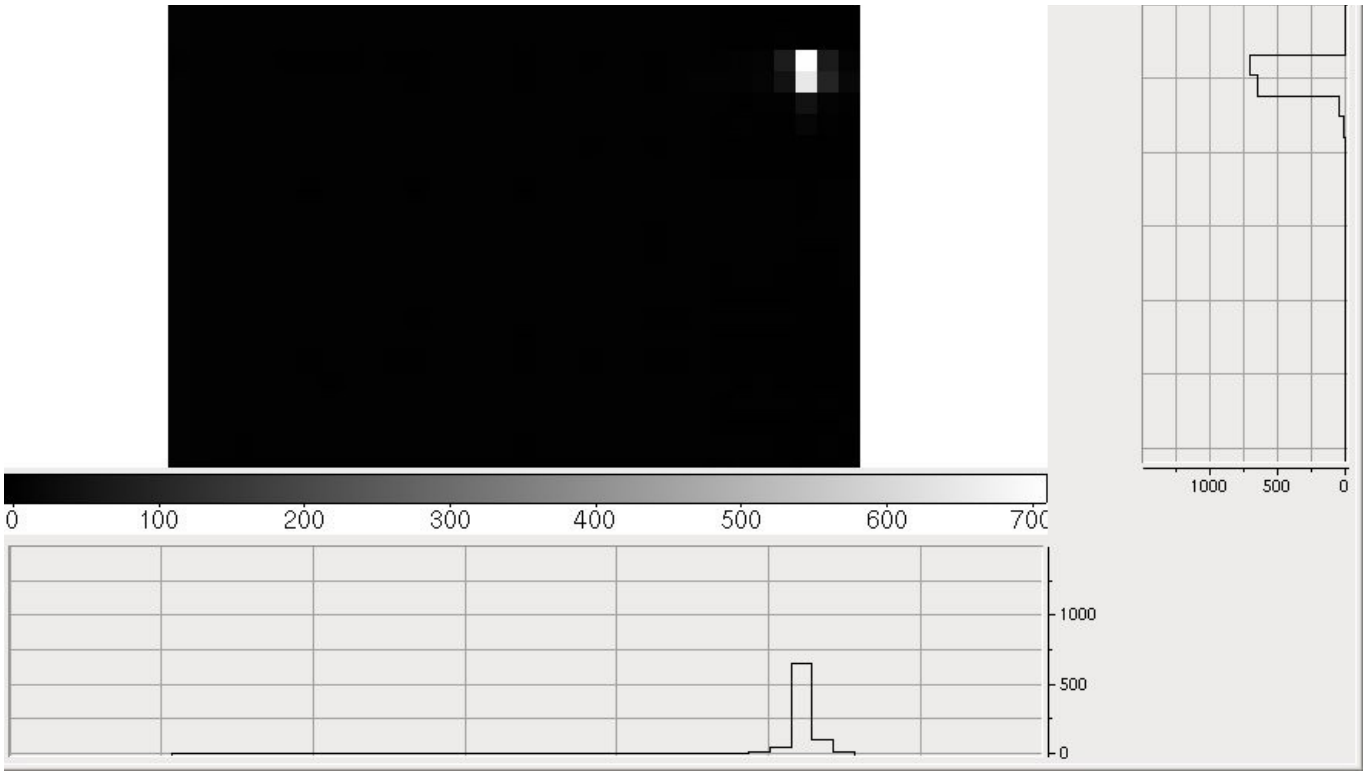
Scan performed with a monochromatic beam of 8 keV, 30 x 30 μm^2 beam size and with 10 μm step.

Raster scans



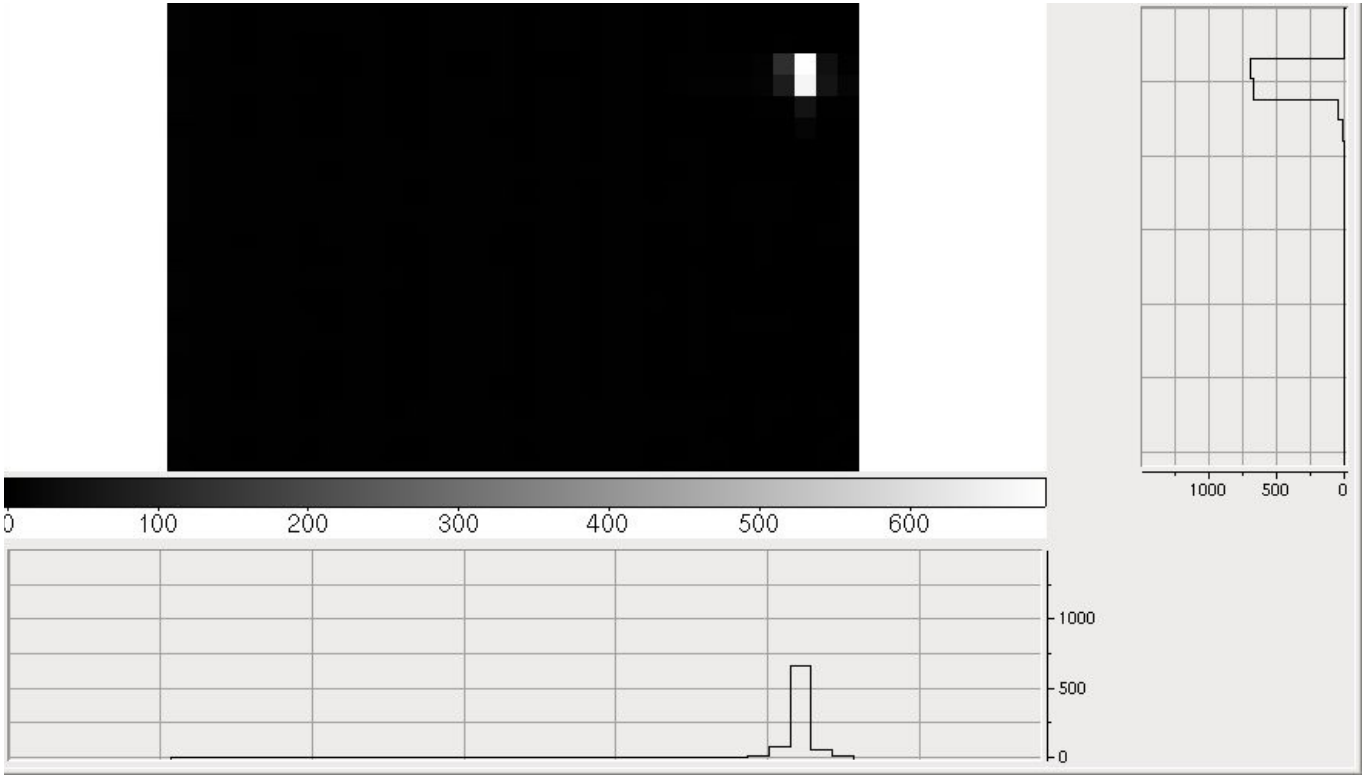
Scan performed with a monochromatic beam of 8 keV, 30 x 30 μm^2 beam size and with 10 μm step.

Raster scans



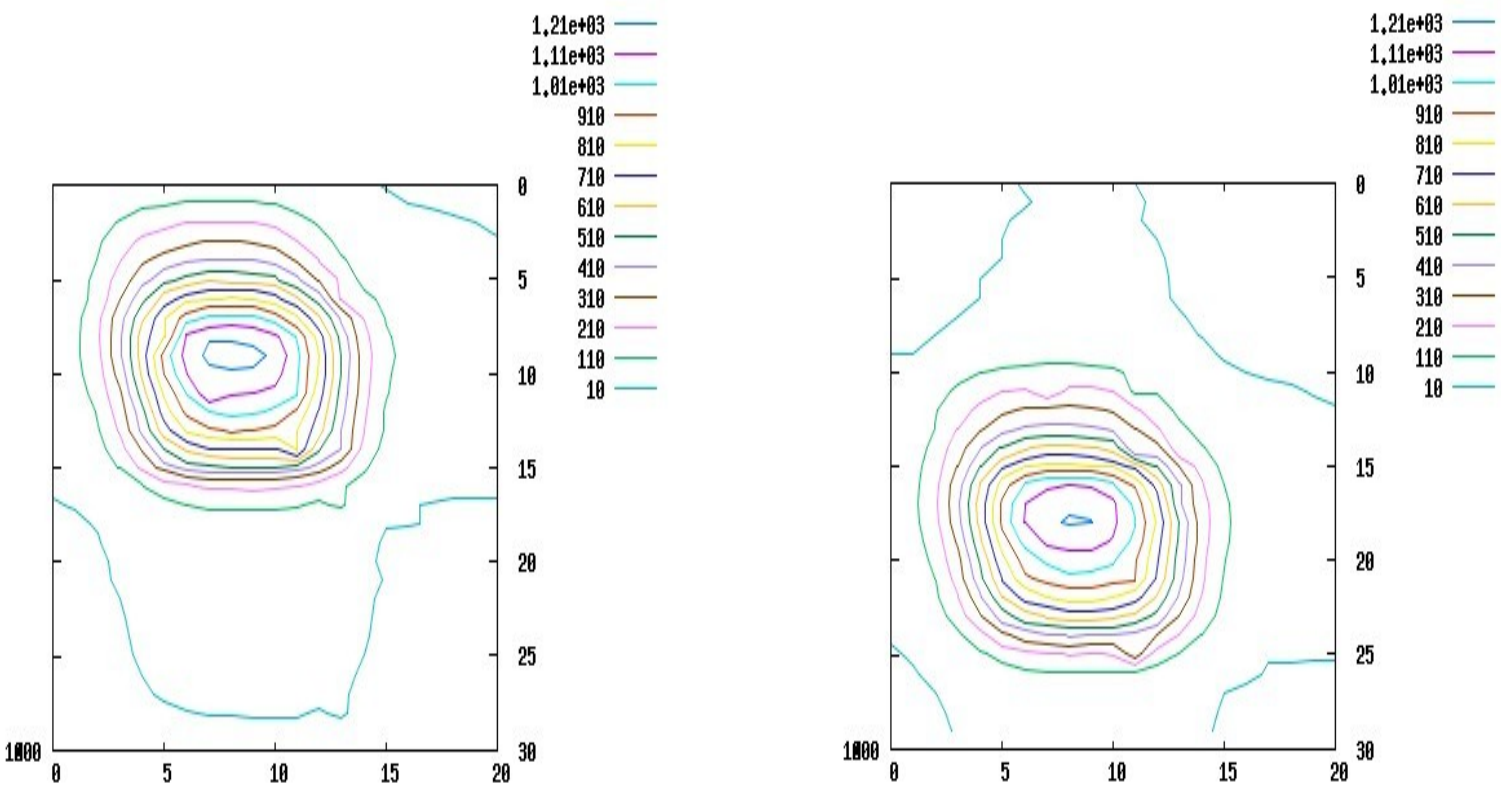
Scan performed with a monochromatic beam of 8 keV, 30 x 30 μm^2 beam size and with 10 μm step.

Raster scans



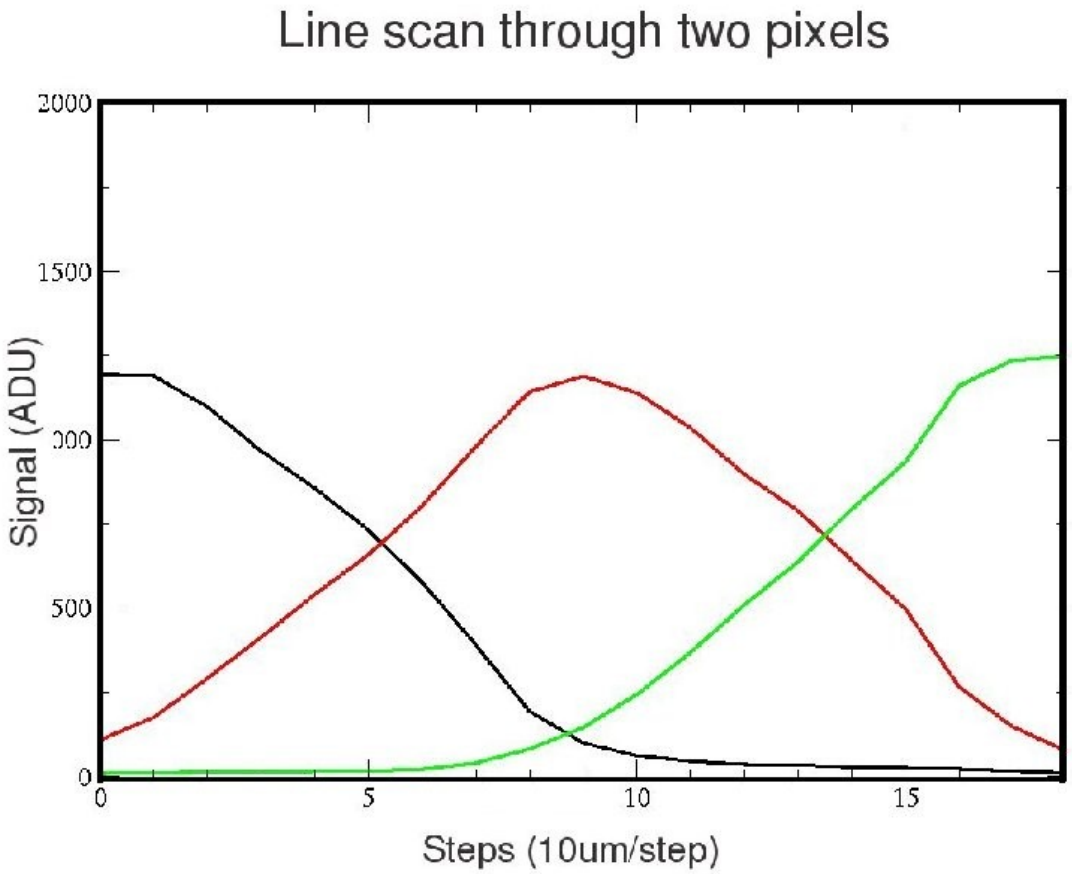
Scan performed with a monochromatic beam of 8 keV, 30 x 30 μm^2 beam size and with 10 μm step.

Contours - Scans



2 adjacent pixels: scan performed in a 300 x 300 μm^2 area with a monochromatic beam of 8 keV, 30 x 30 μm^2 beam size, 10 μm step and 8 ms integration time.

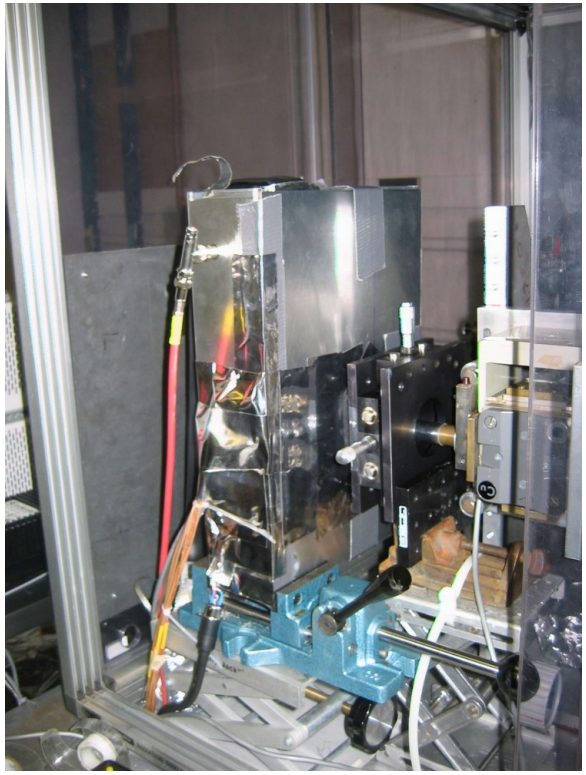
1D-Scans

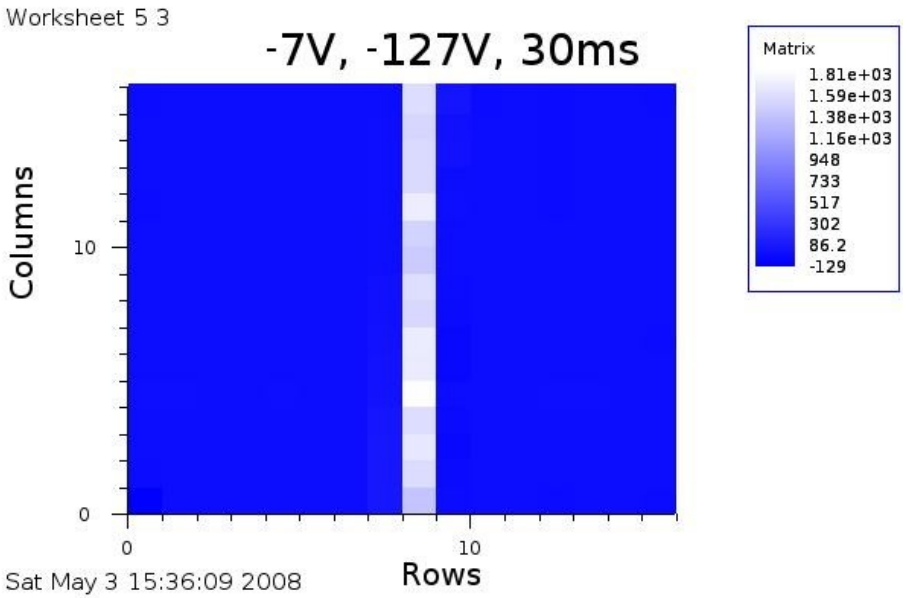


Scan across 2 pixels with a monochromatic beam of 8 keV, 30 x 30 μm^2 beam size and with 10 μm step.

X-ray tube setup – 2D map

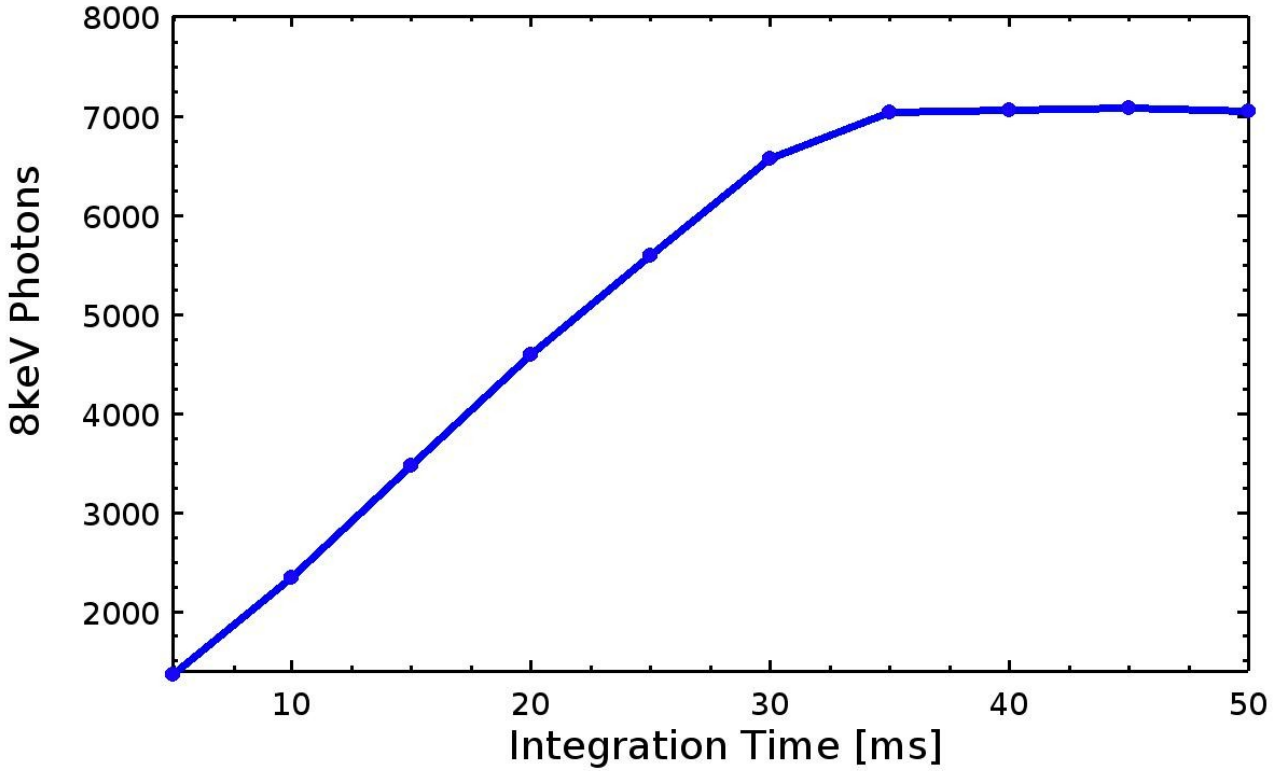
Cu k-alpha





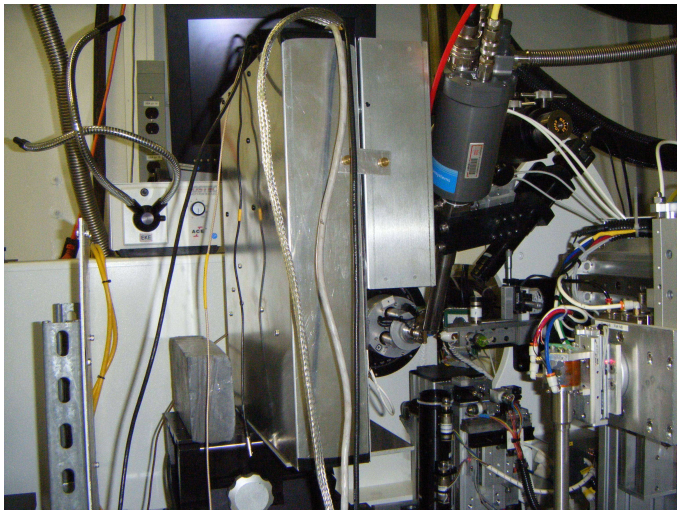
Measurements performed with X-ray generator at 20 KV and 5 mA, with a 25 µm slit. The data is double correlated background subtracted with exponential filter, ADC 2V / 4096, Amp gain = ~ 0.3 mV/fC.

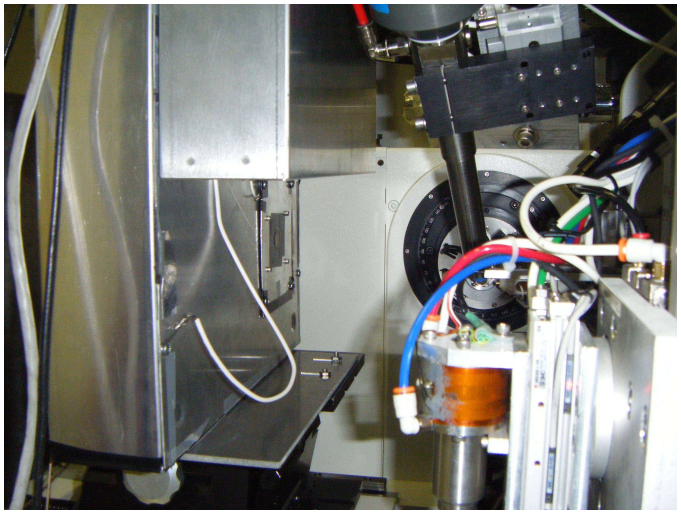
Linearity – Full well

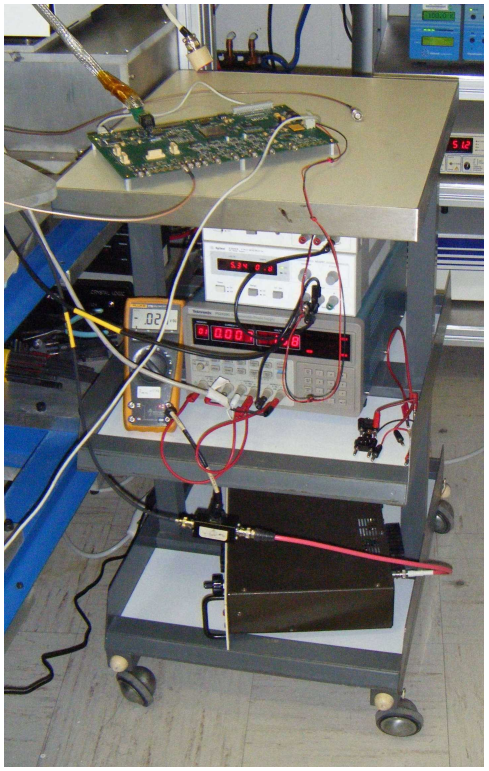


Number of photons as function of the integration time for a pixel at the Cu k-alpha.

Let's give it a try!

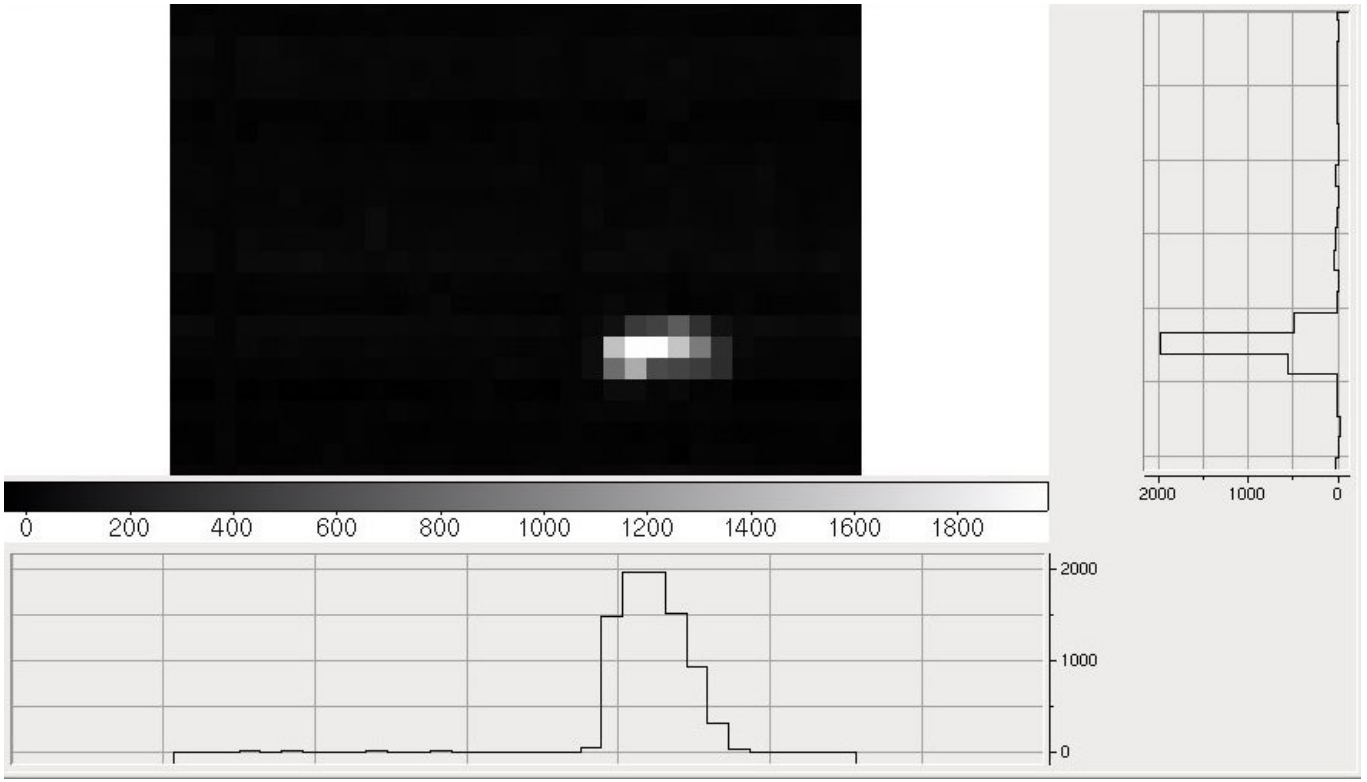






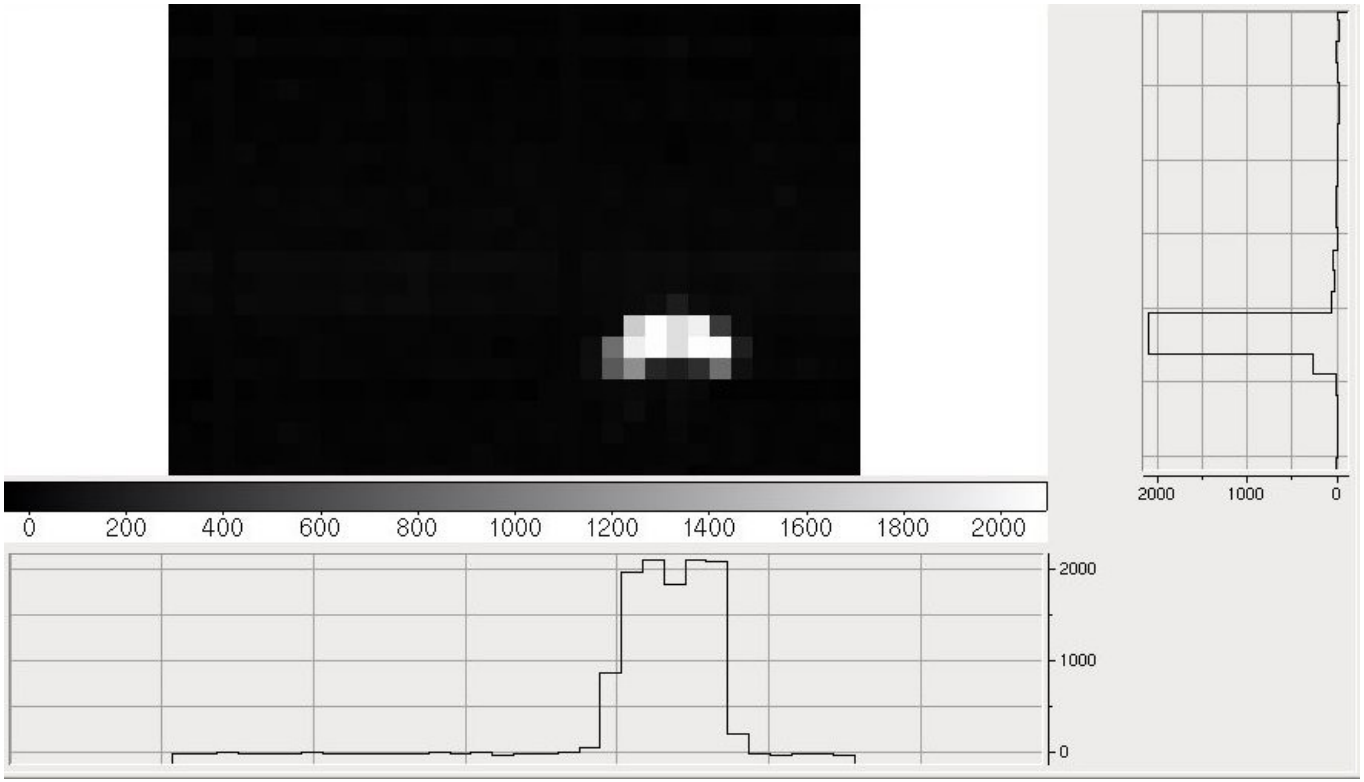
X6A
Beam energy = 12.2keV
Beam size @ sample = 200μm x 200μm
Sample: Thaumatin

X6A - Thaumatin



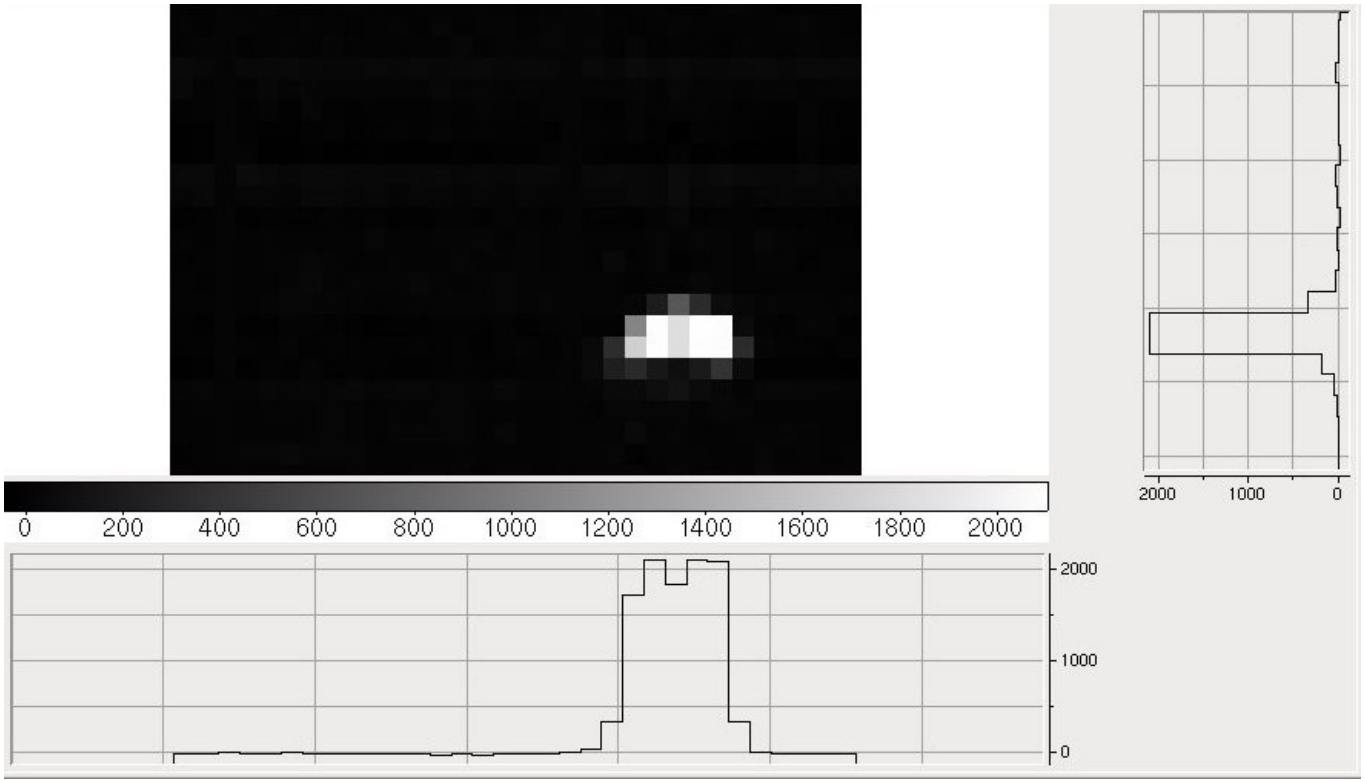
Rotation 0.5° / s – Integration 32 ms / frame

X6A - Thaumatin



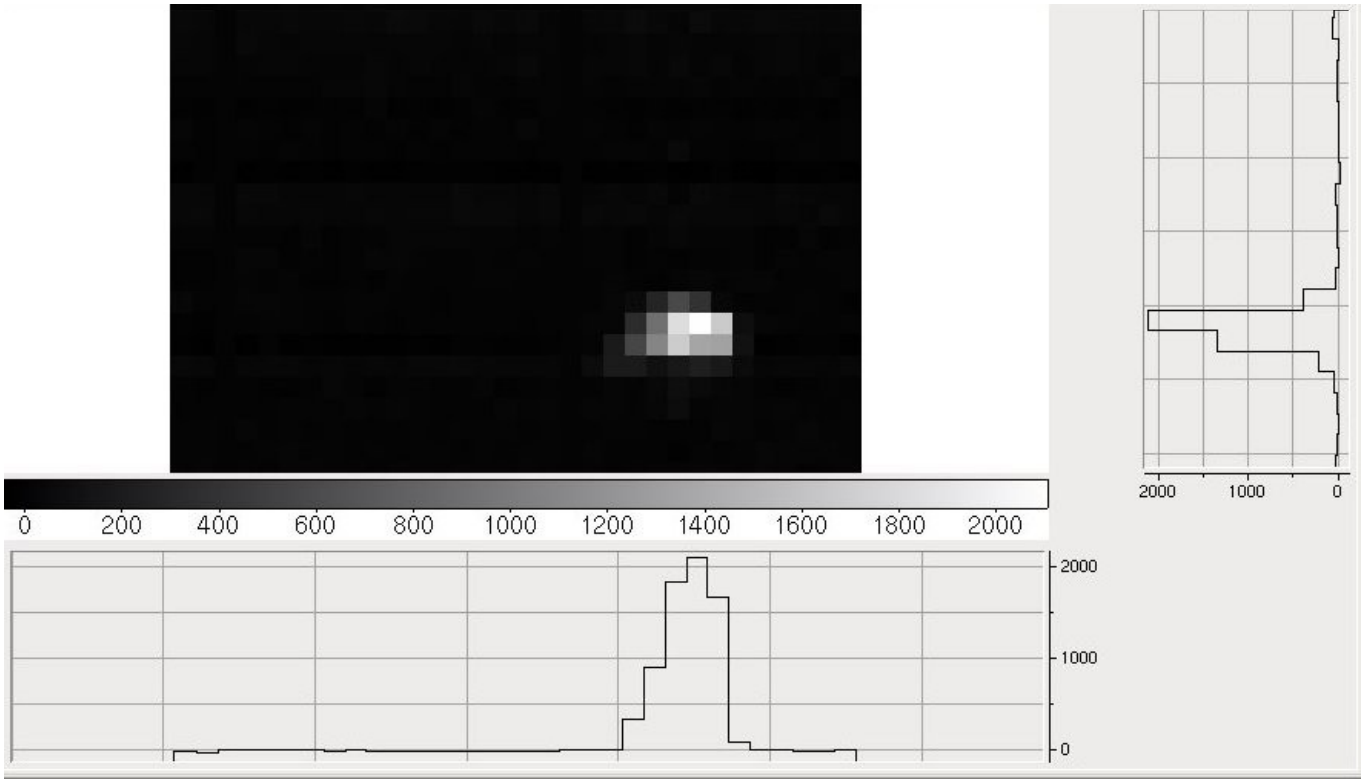
Rotation 0.5° / s – Integration 32 ms / frame

X6A - Thaumatin



Rotation 0.5° / s – Integration 32 ms / frame

X6A - Thaumatin



Rotation 0.5° / s – Integration 32 ms / frame

Summary

- Fabrication processing established.
- Preliminary results: promising.
- Tests: constraints dictated by available readout systems.
- ASIC is currently being tested.
- Tiling under development.

Contributions

Peter Siddons, Tony Kuczwesky, Rich Mitcha (NSLS, BNL)

Pavel Rehak, Wei Chen, Zheng Li (Instr. Div.,BNL)

Angelo Dragone (NSLS, BNL - SLAC)

Jack Fried, Jean-François Pratte (Instr. Div., BNL)

Jean Jakoncic (NSLS, BNL)

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- Vivian Stojanoff
- Tony Bollinger
- Abdel Isakovic

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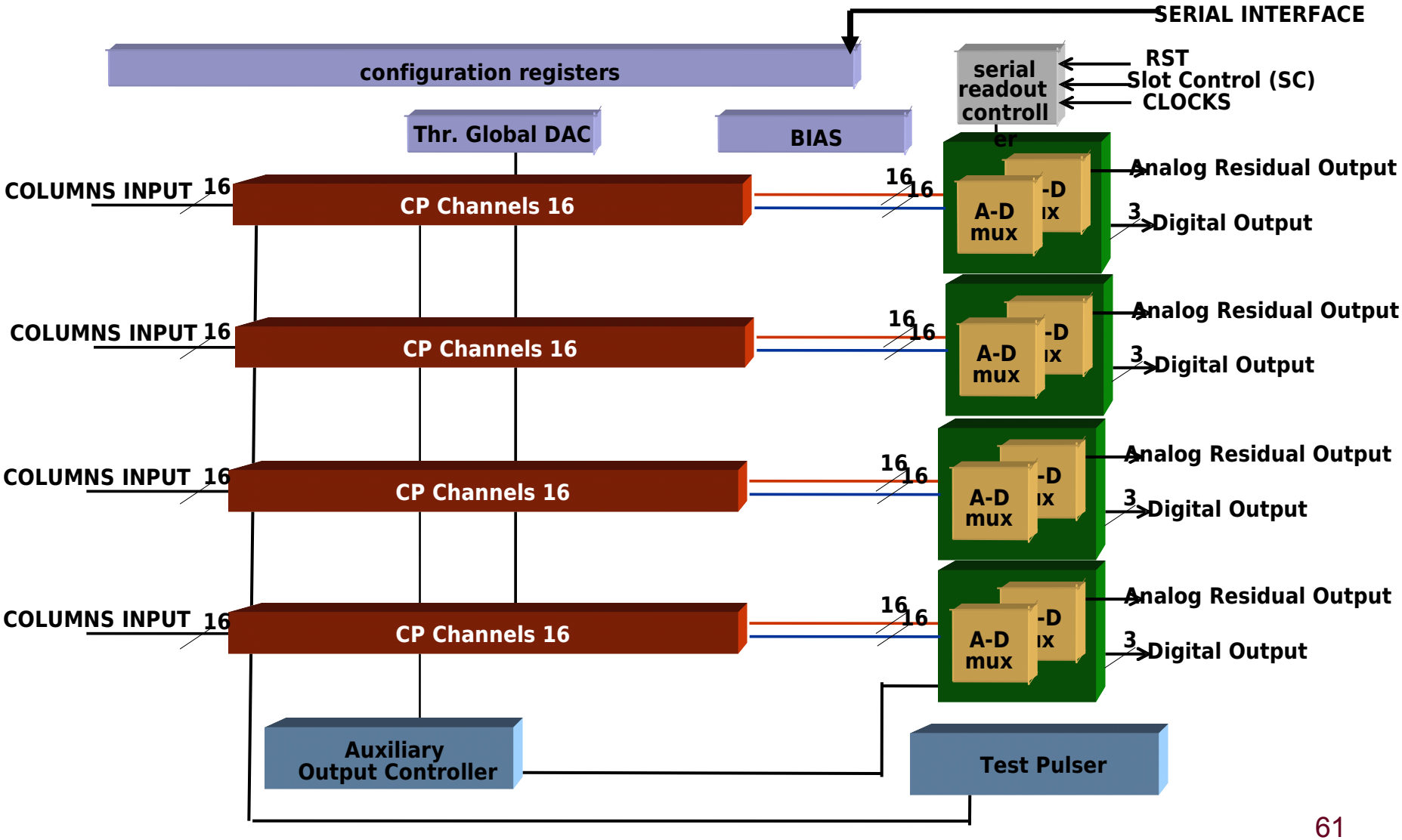
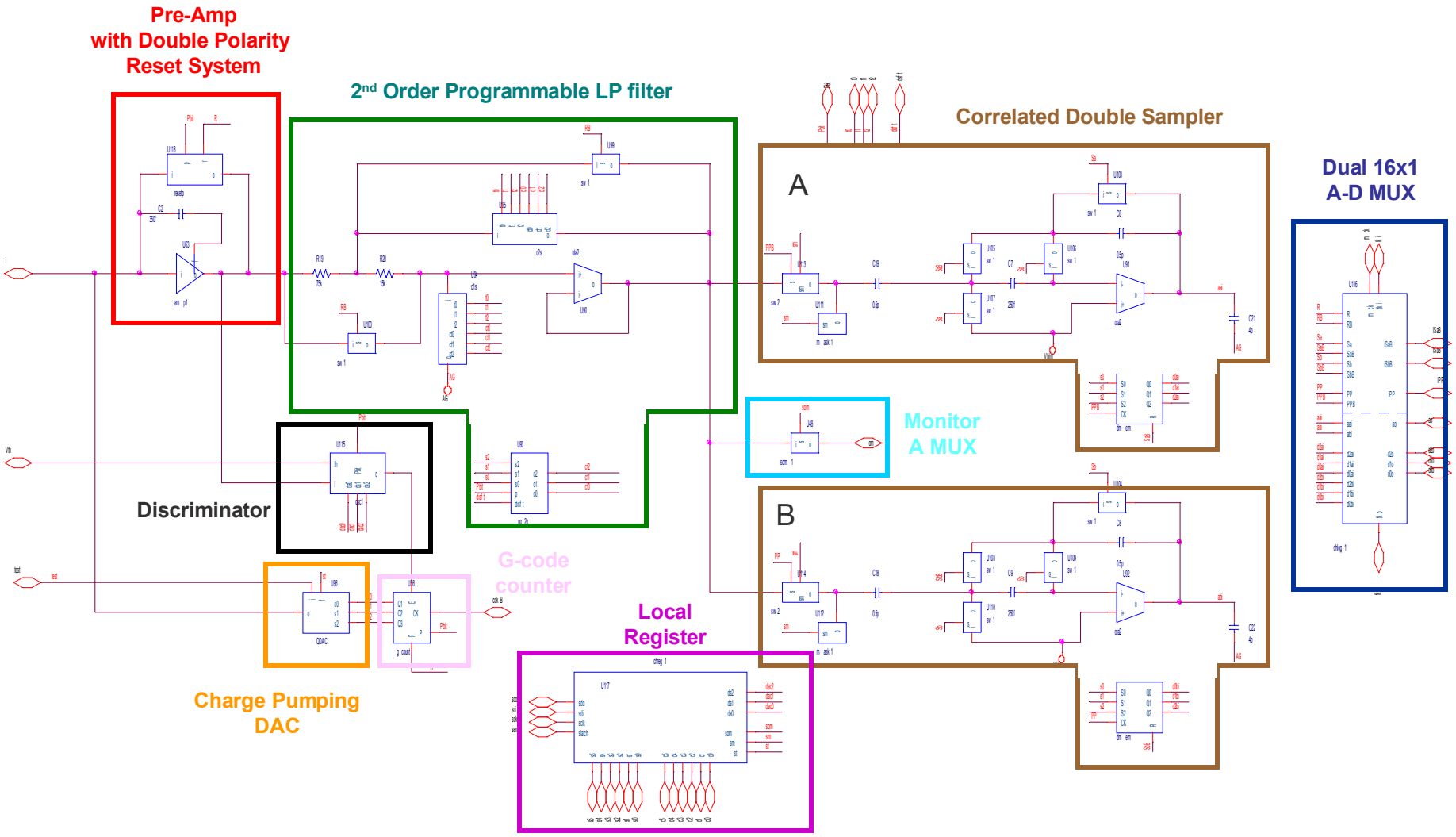
Thank you!

Backups

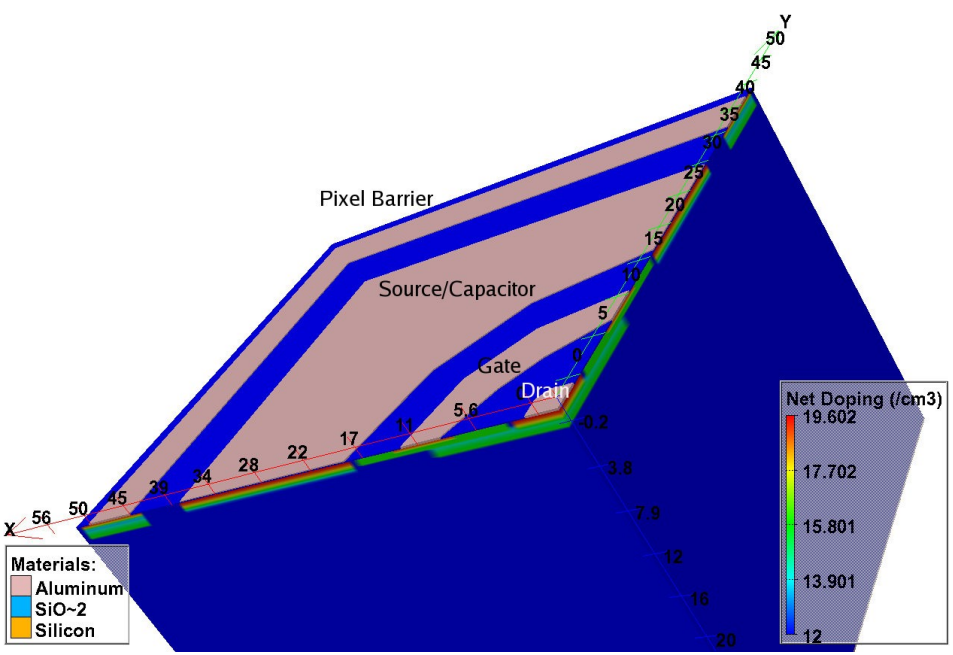
ASIC architecture

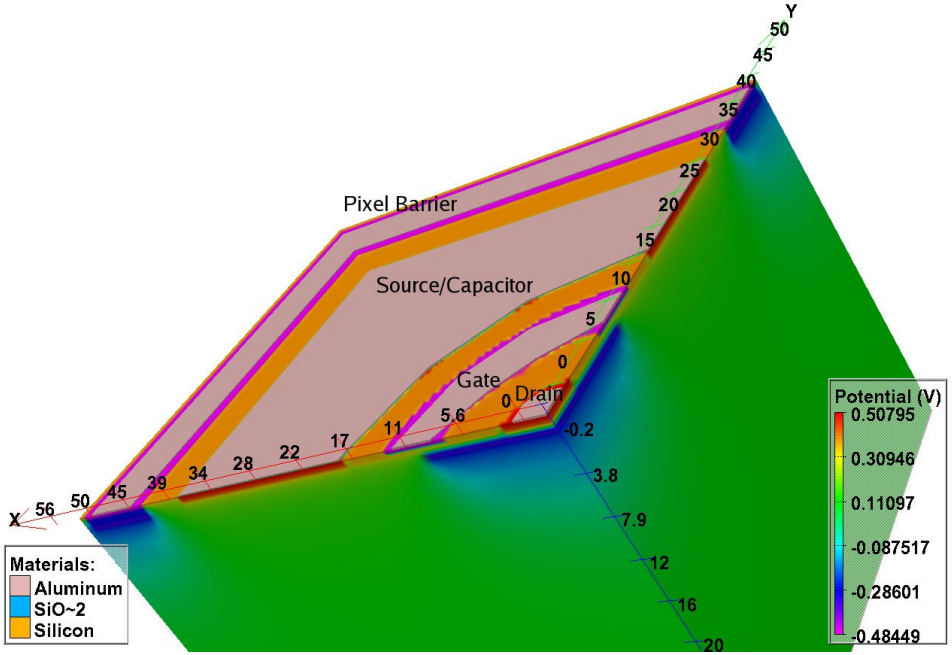


Charge Pump Channel



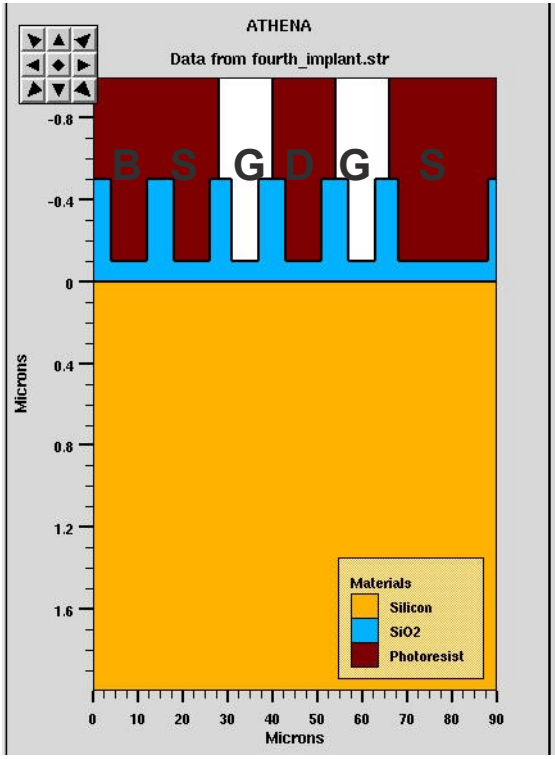
Pixel simulations: 3D cross sections

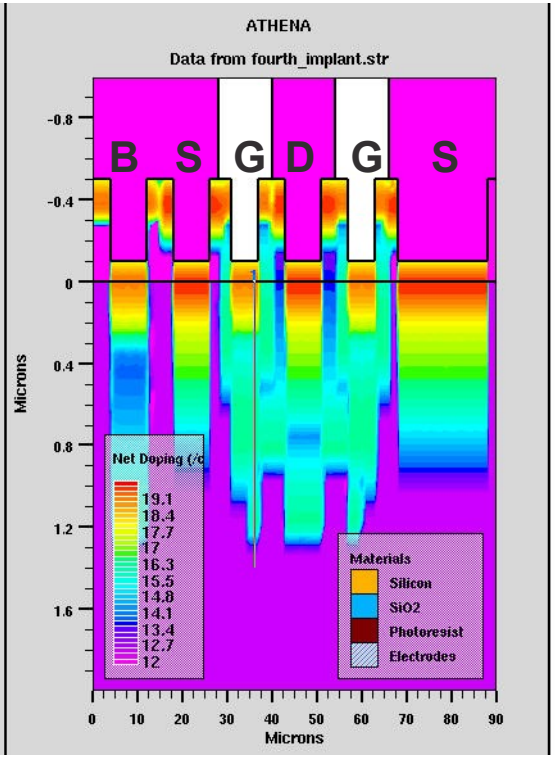


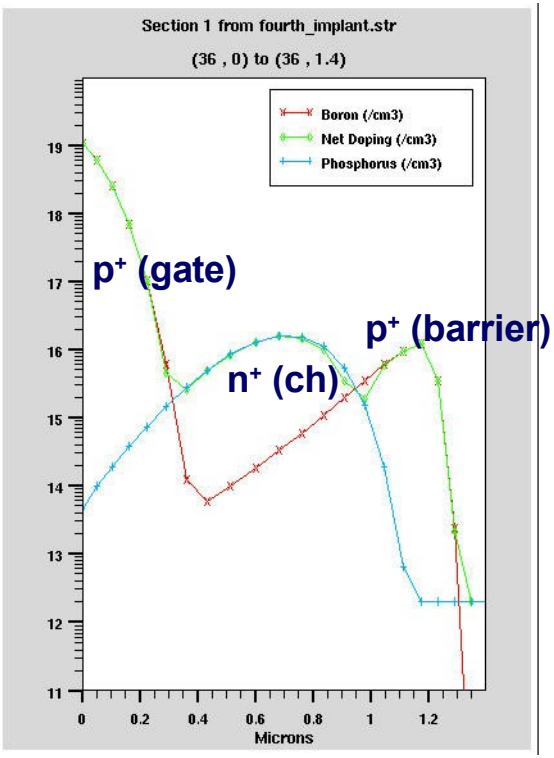


Results from SILVACO - ATLAS simulations. 3D view of a pixel section.
This structure, showing the net doping (left) and built-in potentials (right).

Implants in device side





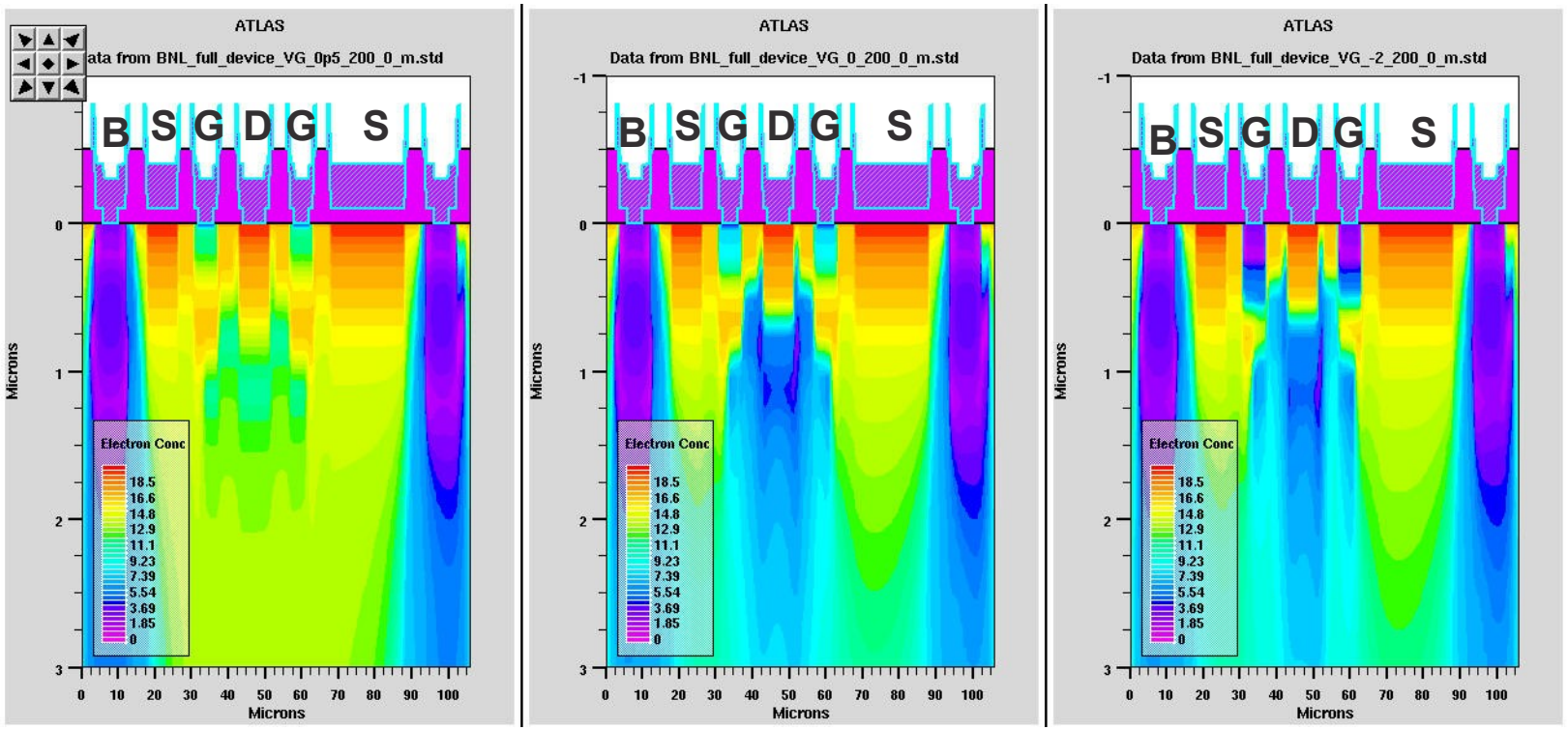


Electron concentration

V_{Gate}=0.5V
OPEN

V_{Gate}=0V

V_{Gate}=-2V
CLOSE



V_{Drain}=0V, V_{Source}=0V, V_{Ch_bar}=-3V, $V_{Backside}$=-200V